

VNKA E

Rosetta 10AN/10ANG

LA-9868P REV 1.0 Schematic

AMD KABINI Quad Core 25W only for UMA
AMD KABINI Quad Core 15W for DIS&UMA
2013-03-18 Rev 1.0

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				Document Number	
				LA-9868P	
Date: Thursday, May 16, 2013				Sheet 1 of 42	

AMD GPU

AMD Sun Pro M2, 64bit with 1GB DDR3(2Gbit)
AMD Sun Pro M2, 64bit with 2GB DDR3(4Gbit)

page 12~19

PCIe Gen2 X4
5Gbps

LVDS/eDP Conn

page 20

DP0 X4

HDMI Conn
(1.4b & 3D)

page 21

DP1 X4

CRT Conn

page 22

DAC

PCIeMini Card For WLAN

PCIe port 2
page 23

PCIe Gen1 X1
APU SMBUS
2.5bps

RTL8106E 10/100M

PCIe port 1
page 25

PCIe Gen1 X1
2.5bps

SPI BUS
3.3V 33HZ

SPI ROM
(4MB)

page 7

APU SMBus

LPC Bus
3.3V 33 MHz

ENE KB9012

page 29

EC SMBus

Touch Pad
page 30

Int.KBD
page 30

G-Sensor
page 25

Memory BUS(DDRIII)
Single Channel

1.5V DDRIII 1333/1600 MT/s
APU SMBUS

200pin DDRIII-SO-DIMM X2

BANK 0, 1, 2, 3 page 10, 11

USB 2.0 Left
USB port 0
page 25

TouchScreen
USB port 4
page 20

Cardreader
USB port 2
page 28

PCIeMini Card
For BT

USB Right1
USB2.0 port 8
page 24

USB Right2
USB2.0 port 9
page 24

Int. Camera
USB port 3
page 20

USB port 1
page 23

USB 2.0
5V 480Mbps

USB Right1
USB3.0 port 0
page 24

USB Right2
USB3.0 port 1
page 24

USB 3.0
5V 5Gbps

SATA port 0
5V 6Gbps

SATA HDD
SATA port 0
page 23

SATA port 1
5V 6Gbps

SATA ODD
SATA port 1
page 23

HD Audio
3.3V 24MHz

HDA Codec
ALC259
page 26

SPK Conn
page 27

JPIO
(HP & MIC)
page 27

Touch Screen Control/B
page 20

DC/DC Interface CKT.
page 31

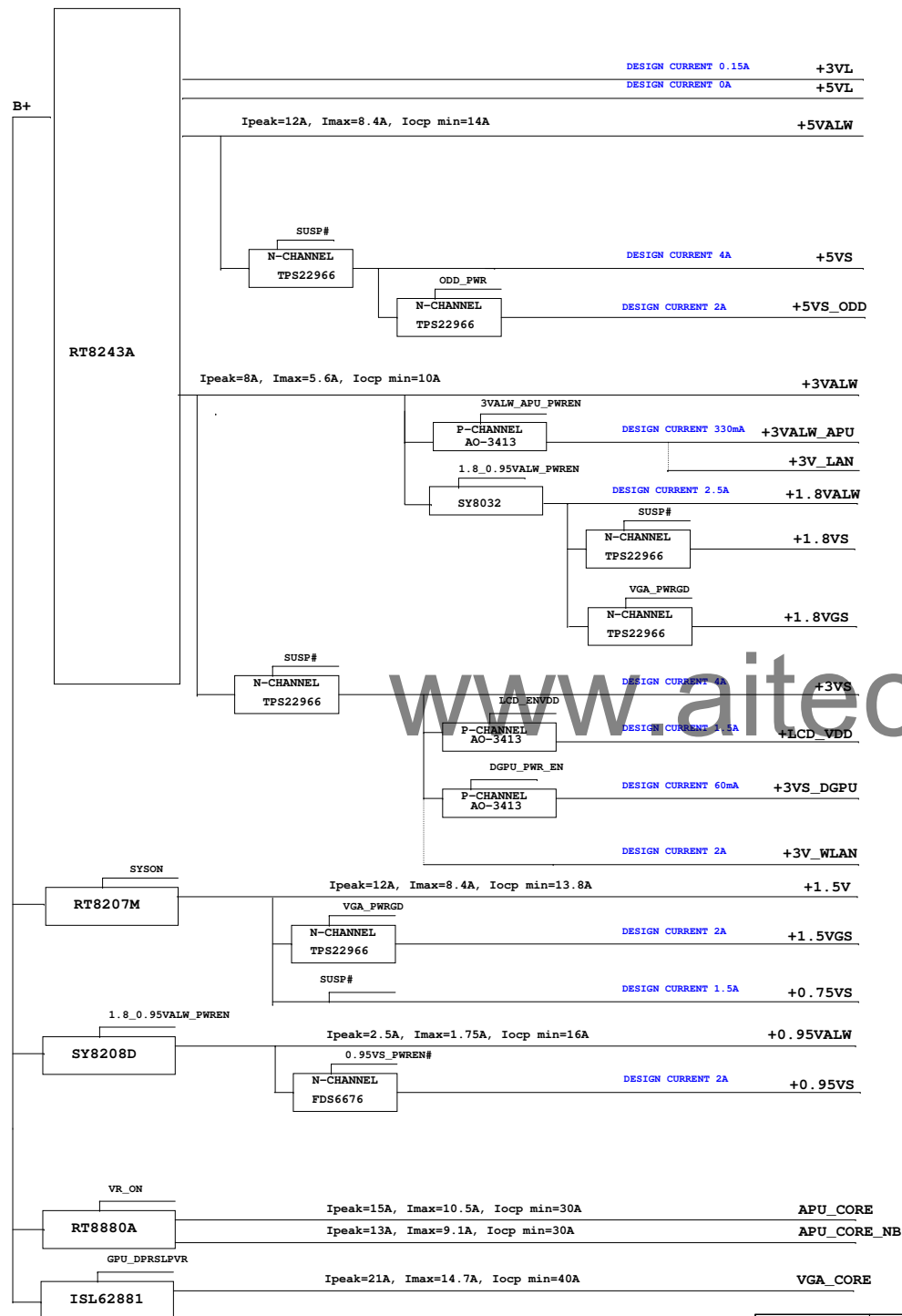
Power Circuit DC/DC
page 32~41

USB2.0&LAN/B
page 25

Power On/Off CKT & Power/B
page 30

RTC CKT.
page 9

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					LA-9868P	1.0
				Date	Thursday, May 16, 2013	Sheet 2 of 42



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				Rev	1.0
				Date	Thursday, May 16, 2013
				Sheet	3 of 42

Voltage Rails

(O MEANS ON X MEANS OFF)

UMA

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.8VALW +0.95VALW +VSB	+1.5V	+5VS +3VS +0.95VS +1.8VS +1.5VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function								
description								
explain								
BTO								

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

APU SM Bus Address (SCL0/SDA0)

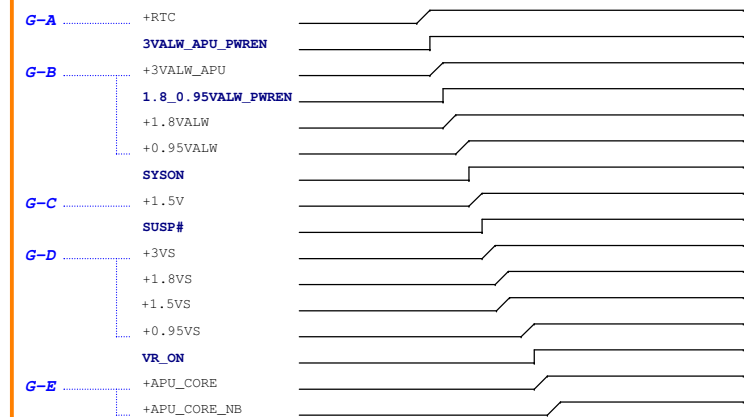
Power	Device	HEX	Address
+3VS	DDR SO-DIMM A	A0H	1010 0000 b
+3VS	DDR SO-DIMM B	A2H	1010 0010 b
+3VS	WLAN		

EC SM Bus1 Address

EC SM Bus2 Address

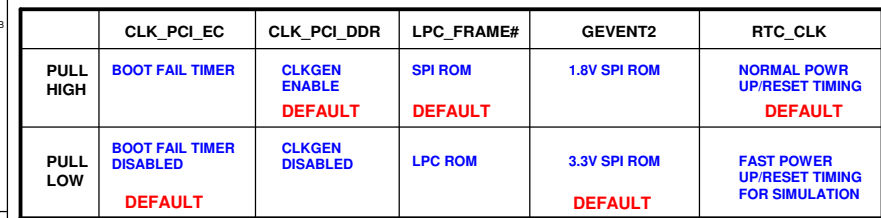
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16H	0001 0110 b	+3VS	G-Sensor	40H	0100 0000 b
+3VL	Charger	12H	0001 0010 b	+3VS	VGA thermal	82H	1000 0010 b
				+3VS	APU thermal	98H	1001 1000 b

APU POWER SEQUENCE

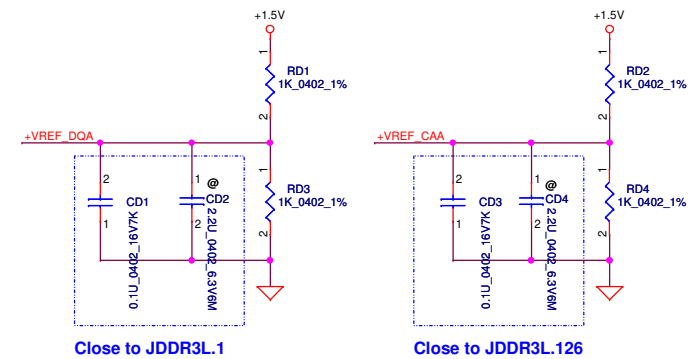
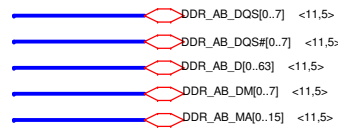


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					Custom	LA-9868P	1.0	
					Date:	Thursday, May 16, 2013	Sheet	4 of 42

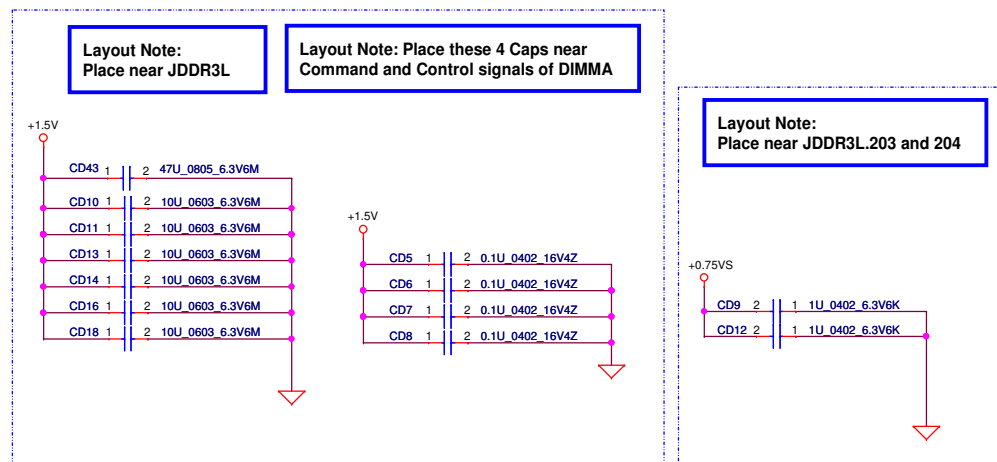
STRAP PINS



SO-DIMM VREF

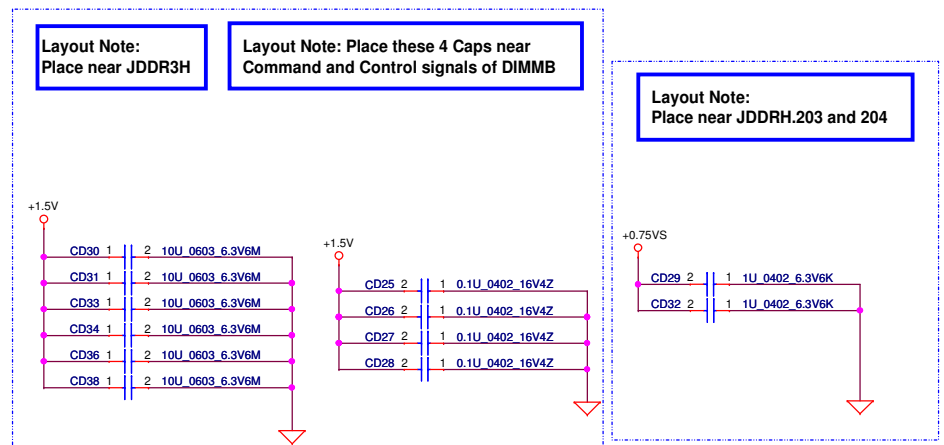
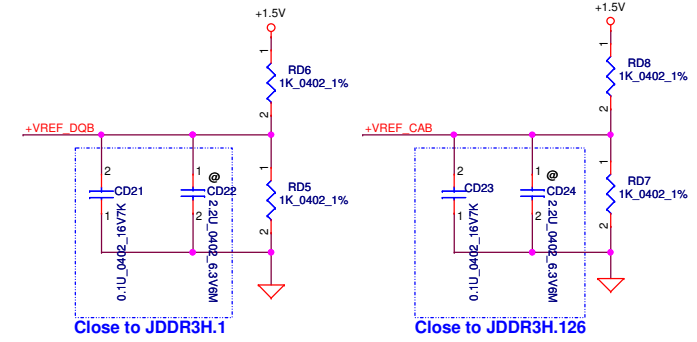


```
DDR_A_CLKI#>DDR_A_CLKI#<5>
DDR_AB_BS1>DDR_AB_BS1<11.5>
DDR_AB_RAS#>DDR_AB_RAS#<11.5>
DDR_A_SCS#>DDR_A_SCS#<5>
DDR_A_ODT0>DDR_A_ODT0<5>
DDR_A_ODT1>DDR_A_ODT1<5>
```



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					LA-9868P	1.0	
Date: Thursday, May 16, 2013				Sheet	10	of 42	

DDR_B_CLK1# DDR_B_CLK1# <-5>
DDR_B_CLK1# DDR_B_CLK1# <-5>
DDR_AB_BS1# DDR_AB_BS1 <-10.5>
DDR_AB_RAS# DDR_AB_RAS# <-10.5>
DDR_B_SCS0# DDR_B_SCS0# <-5>



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					LA-9868P
				Date:	Thursday, May 16, 2013
				Sheet	11 of 42

<5> PCIE_ATX_C_GRX_P[3..0] PCIE_ATX_C_GRX_P[3..0]
<5> PCIE_ATX_C_GRX_N[3..0] PCIE_ATX_C_GRX_N[3..0]

UV1A

PART 1 OF 9

PCIE GTX_C_ARX_P[3..0] PCIE GTX_C_ARX_P[3..0] <5>
PCIE GTX_C_ARX_N[3..0] PCIE GTX_C_ARX_N[3..0] <5>

PCIE_ATX_C_GRX_P0 AA38 PCIE_RX0P
PCIE_ATX_C_GRX_N0 Y37 PCIE_RX0N

PCIE_ATX_C_GRX_P1 Y35 PCIE_RX1P
PCIE_ATX_C_GRX_N1 W38 PCIE_RX1N

PCIE_ATX_C_GRX_P2 W38 PCIE_RX2P
PCIE_ATX_C_GRX_N2 Y37 PCIE_RX2N

PCIE_ATX_C_GRX_P3 V35 PCIE_RX3P
PCIE_ATX_C_GRX_N3 U38 PCIE_RX3N

U38 PCIE_RX4P
T37 PCIE_RX4N

T35 PCIE_RX5P
R36 PCIE_RX5N

R38 PCIE_RX6P
P37 PCIE_RX6N

P35 PCIE_RX7P
N36 PCIE_RX7N

N38 NC
M37 NC

M35 NC
L36 NC

L38 NC
K37 NC

K35 NC
J36 NC

J38 NC
H37 NC

H35 NC
G36 NC

G38 NC
F37 NC

F35 NC
E37 NC

CLOCK

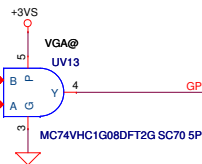
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<7> CLK_PCIE_VGA# CLK_PCIE_VGA# AA36 PCIE_REFCLKN

RV2 2 VGA@ 1 AH16 TEST_PG
RV2 1K_0402_5%

3.3-V tolerant GPU_RST# AA30 PERSTB

VGA@ RV212 100K_0402_5%

<8> PXS_RST# GPU_RST#
<23,25,8> APU_PCIE_RST#



Y33 PCIE GTX_ARX_P0 .1U_0402_16V7K CV1 1 2 VGA@ PCIE GTX_C_ARX_P0
Y32 PCIE GTX_ARX_N0 .1U_0402_16V7K CV2 1 2 VGA@ PCIE GTX_C_ARX_N0

W33 PCIE GTX_ARX_P1 .1U_0402_16V7K CV3 1 2 VGA@ PCIE GTX_C_ARX_P1
W32 PCIE GTX_ARX_N1 .1U_0402_16V7K CV4 1 2 VGA@ PCIE GTX_C_ARX_N1

U33 PCIE GTX_ARX_P2 .1U_0402_16V7K CV5 1 2 VGA@ PCIE GTX_C_ARX_P2
U32 PCIE GTX_ARX_N2 .1U_0402_16V7K CV6 1 2 VGA@ PCIE GTX_C_ARX_N2

U30 PCIE GTX_ARX_P3 .1U_0402_16V7K CV7 1 2 VGA@ PCIE GTX_C_ARX_P3
U29 PCIE GTX_ARX_N3 .1U_0402_16V7K CV8 1 2 VGA@ PCIE GTX_C_ARX_N3

T33 PCIE_TX4P
T32 PCIE_TX4N

T30 PCIE_TX5P
T29 PCIE_TX5N

P33 PCIE_TX6P
P32 PCIE_TX6N

P30 PCIE_TX7P
P29 PCIE_TX7N

N33 NC
N32 NC

N30 NC
N29 NC

L33 NC
L32 NC

L30 NC
L29 NC

K33 NC
K32 NC

J33 NC
J32 NC

K30 NC
K29 NC

H33 NC
H32 NC

AC Coupling Capacitor
PCIEr Gen1 and Gen2 only: Recommended value is 100 nF 10%.
PCIEr Gen3: Recommended value is 220 nF 10%.

LVDS Interface

UV1D

PART 7 OF 9

RSVD/AVARY BL AK27
RSVD/DIGON AJ27

LVDS CONTROL

TXCBP_DPB3P AK35
TXCBM_DPB3N AL36

TX3P_DPB2P AJ38
TX3M_DPB2N AK37

TX4P_DPB1P AH35
TX4M_DPB1N AJ36

TX5P_DPB0P AG38
TX5M_DPB0N AH37

NC#AF35 AF35
NC#AG36 AG36

TXCAP_DPA3P AP34
TXCAM_DPA3N AR34

TX0P_DPA2P AW37
TX0M_DPA2N AU35

TX1P_DPA1P AR37
TX1M_DPA1N AU39

TX2P_DPA0P AP35
TX2M_DPA0N AR35

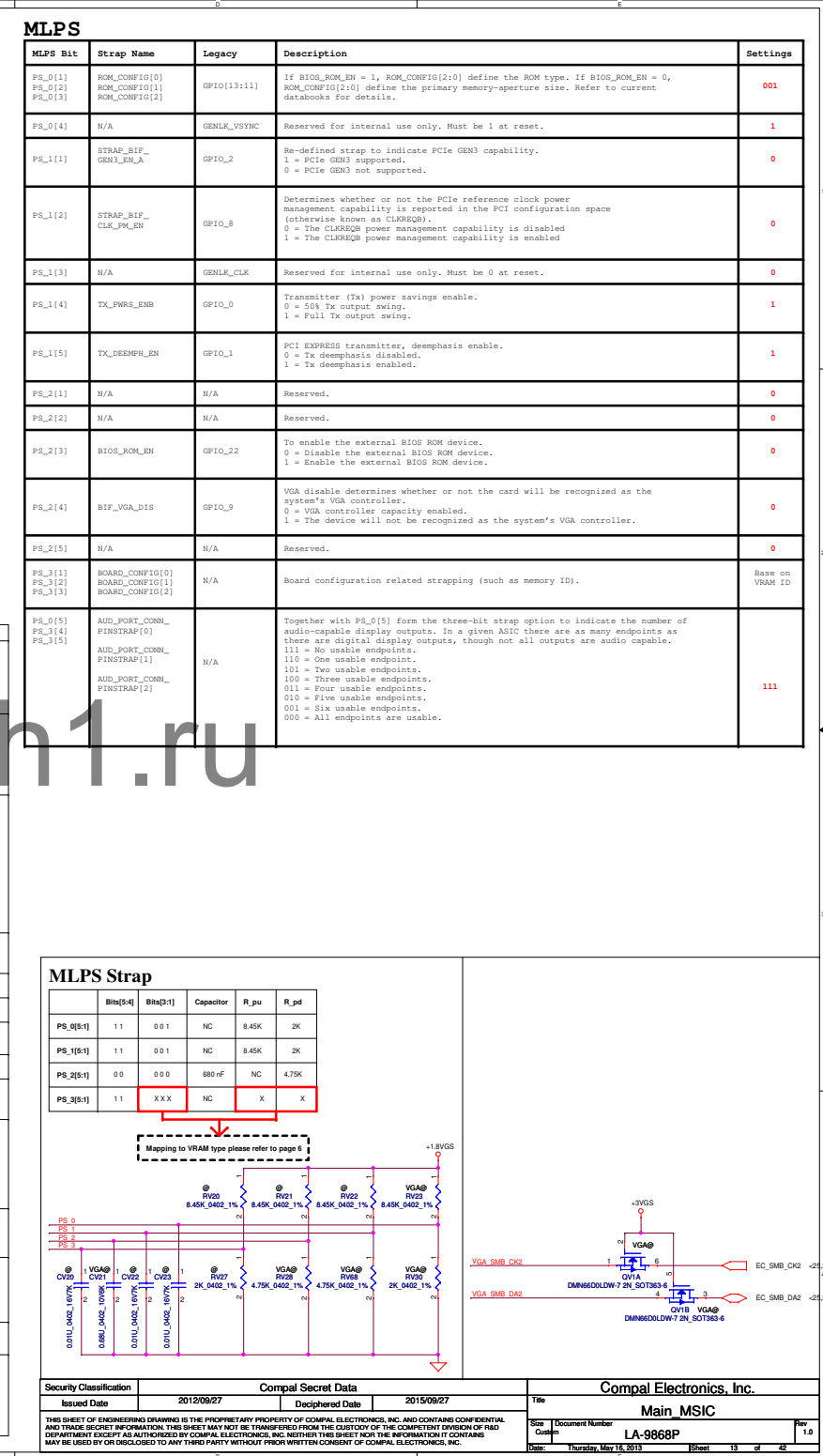
NC AN36
NC AP37

VGA@ SUN-PRO M2_FCBGA962

For MEMCLK 1GHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-107G:K	1.35V/900MHz 1.5V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-BC11	1.5V/900MHz	111	4750	NC

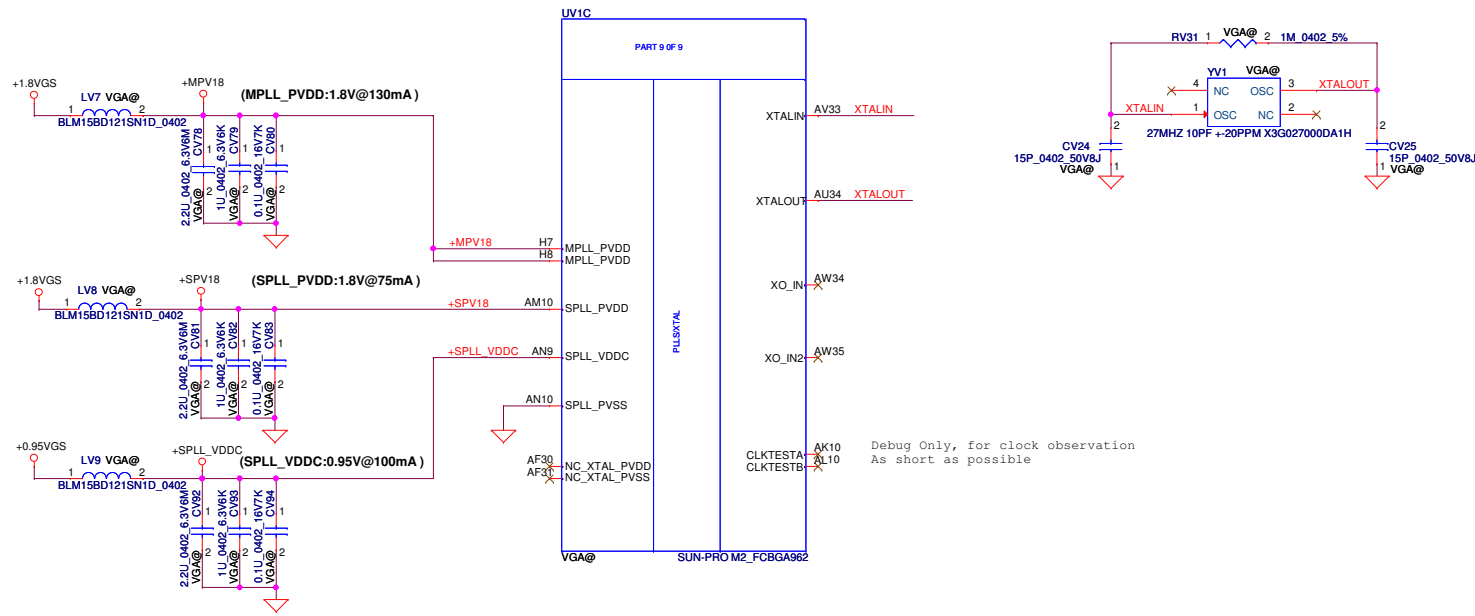
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				Custom	LA-9868P	1.0
				Date	Thursday, May 16, 2013	Sheet 12 of 42



MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

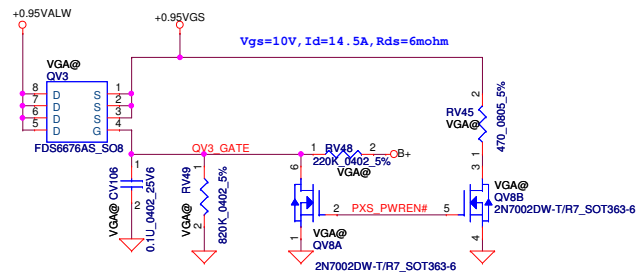
SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

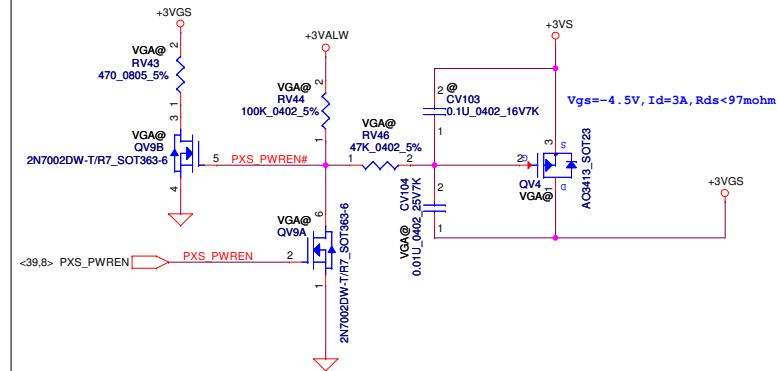


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+0.95VS to +0.95VGS



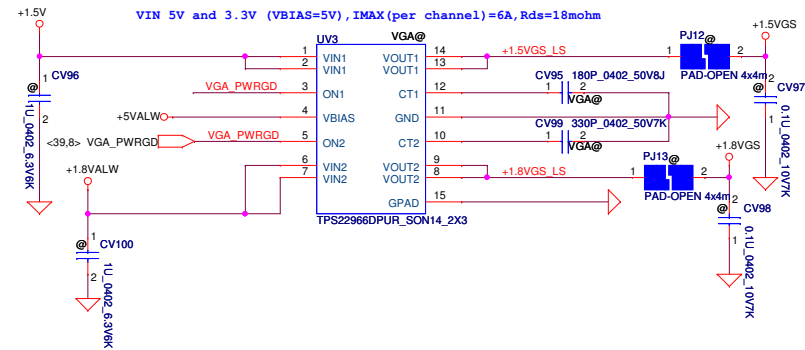
+3VS to +3VGS



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				Rev 1.0
				Date: Thursday, May 16, 2013
				Sheet 14 of 42

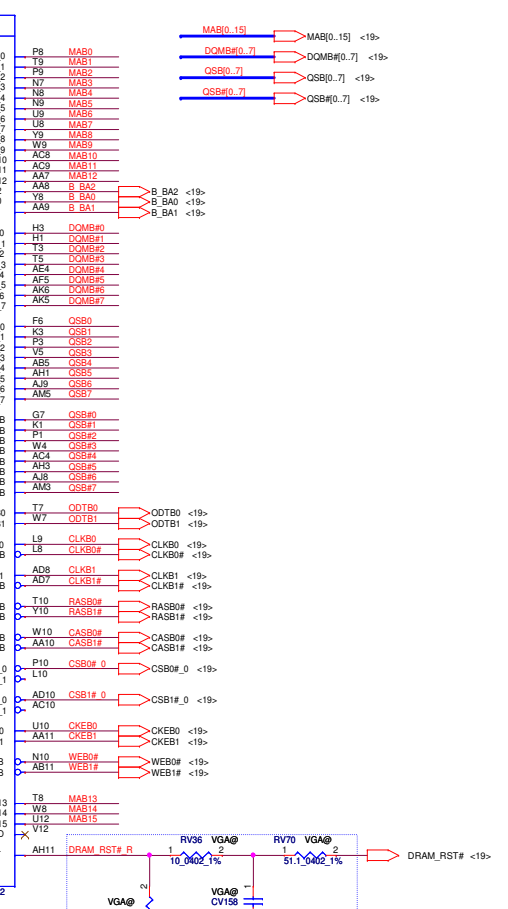
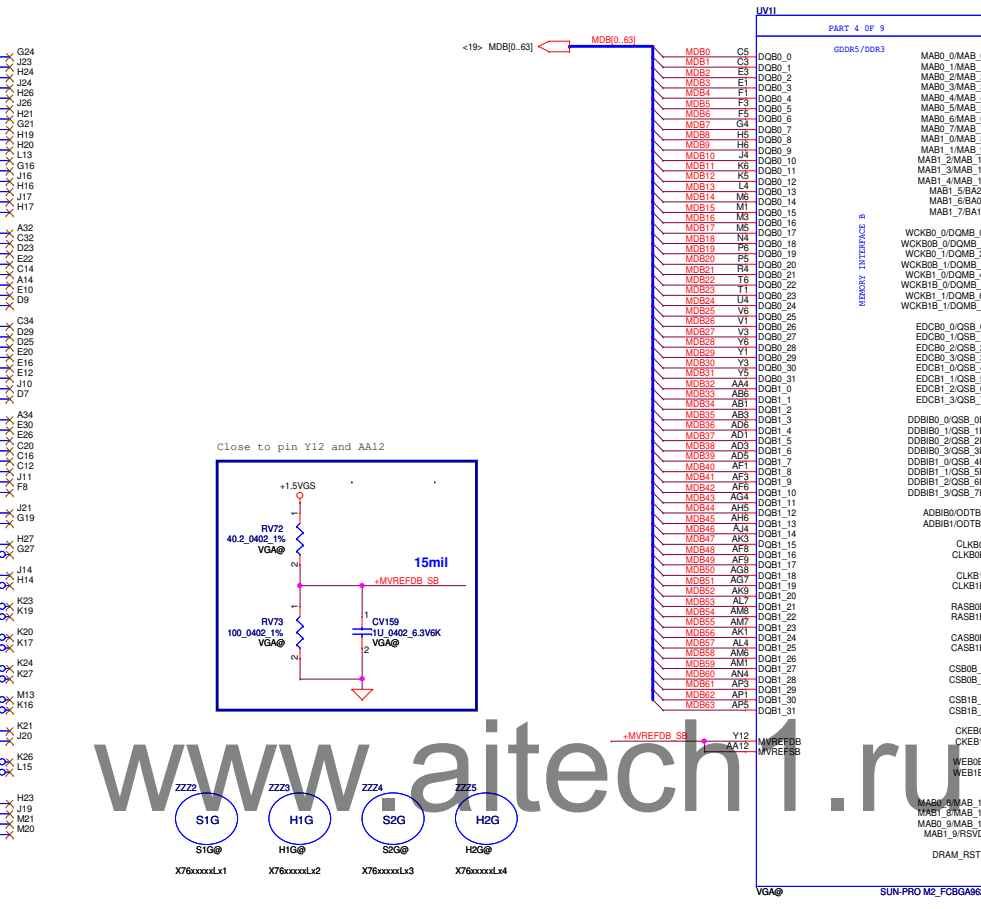
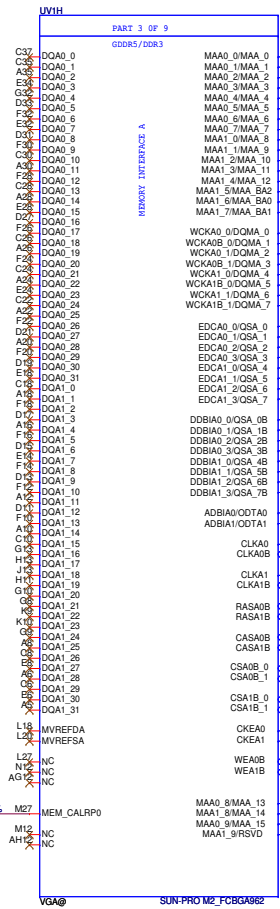
Only for Kabini

+1.8VALW to +1.8VGS
+1.5V to +1.5VGS



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				Revision	Rev 1.0
Date: Thursday, May 16, 2013				Sheet	15 of 42



Memory clock 900MHz RC99 10K pull down

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA00003YO70	H5TQ2G63DFR-11C	X7648051L01	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Micron	SA00005XB00	MT41K128M16JT-107G.K	X7648051L03	2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH00	K4W2G1646E-BC11	X7648051L04	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC

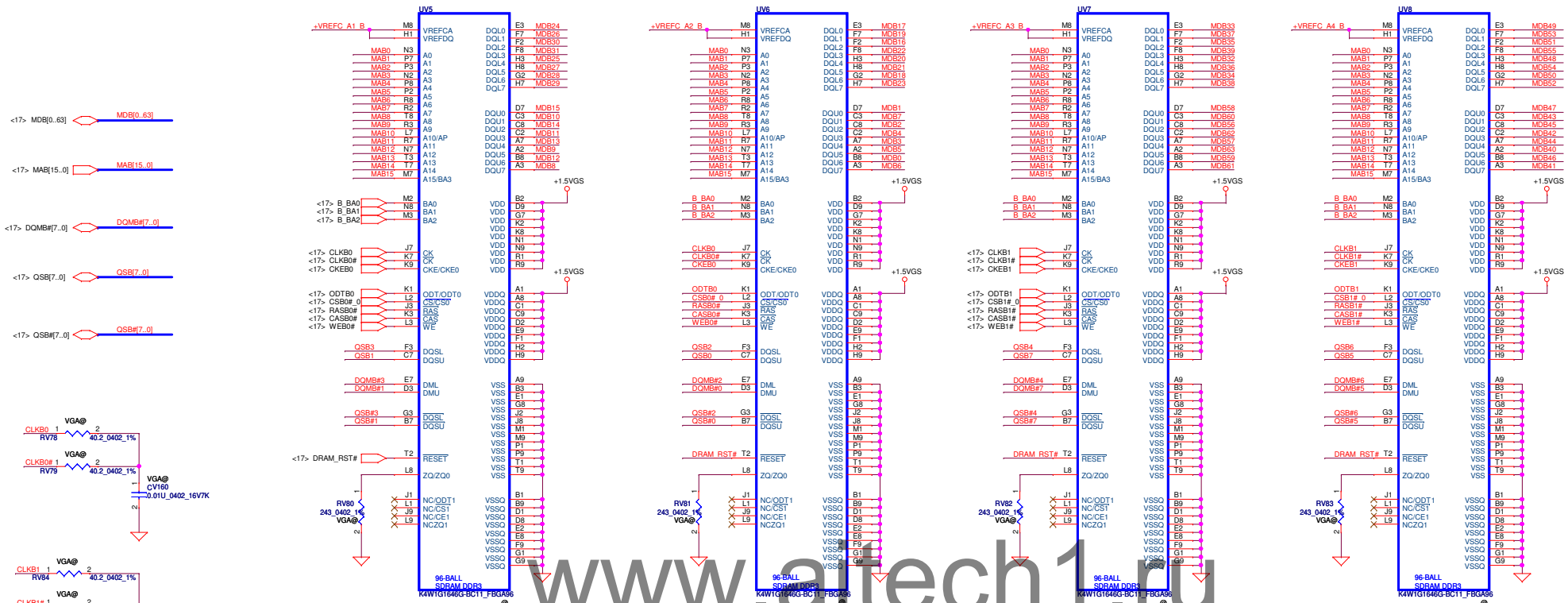
Memory clock 1GHz RC95 10K pull high

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA000065300	H5TQ2G63DFR-N0C	X7648051L02	2Gbit	128M*16	1GB/4pcs	0	1	0	RV20 4.53K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A	X7648051L05	2Gbit	128M*16	1GB/4pcs	1	1	0	RV20 3.4K	RV27 10K

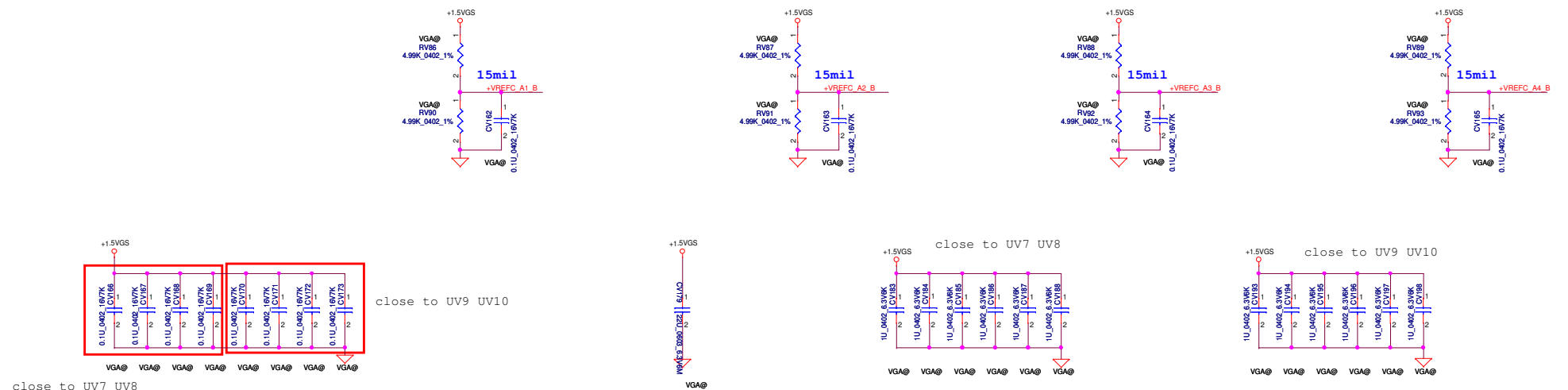


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								Document Number		Rev	
								Custom		1.0	
								LA-9868P			
Date: Thursday, May 16, 2013								Sheet 18 of 42			

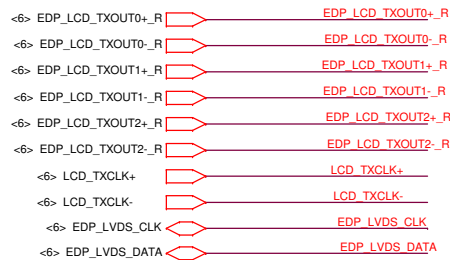
CHANNEL B: 512MB/1024MB DDR3



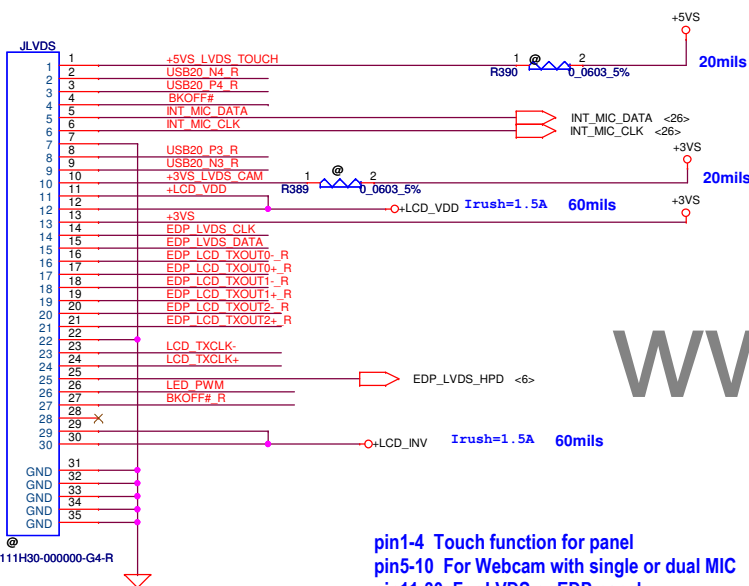
Supported Memory Configurations: Up to 4 Gbit/part for DDR3.



Security Classification	Compal Secret Data			Title	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	VRAM Channel B	
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				LA-9868P	Rev 1.0
				Date: Thursday, May 16, 2013	Sheet 19 of 42



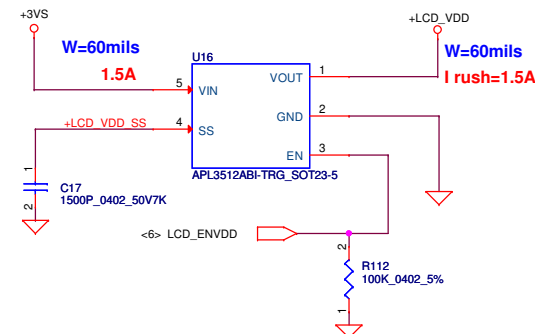
If it's EPD, they're become
 LCD_TXOUT2+_R = EDP_TX0+
 LCD_TXOUT2-_R = EDP_TX0-
 LCD_TXOUT1+_R = EDP_TX1+
 LCD_TXOUT1-_R = EDP_TX1-
 LVDS_CLK = EDP_AUXP
 LVDS_DATA = EDP_AUXN



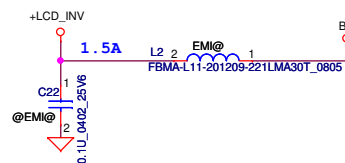
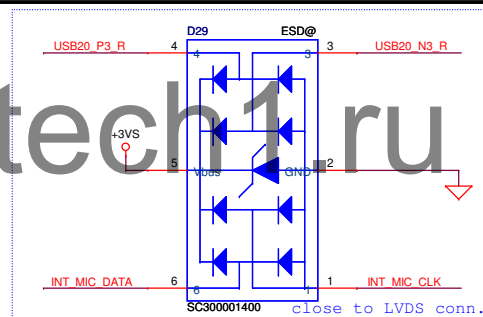
pin1-4 Touch function for panel
 pin5-10 For Webcam with single or dual MIC
 pin11-30 For LVDS or EDP panel

LCD_VDD

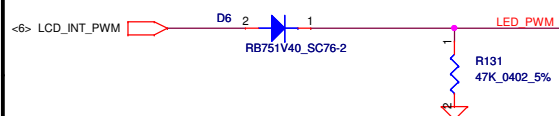
Need check eDP&LVDS both 3V power rail.



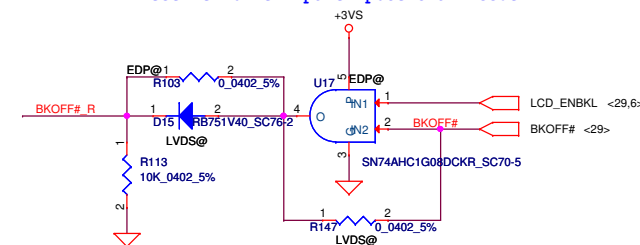
LCD_INV



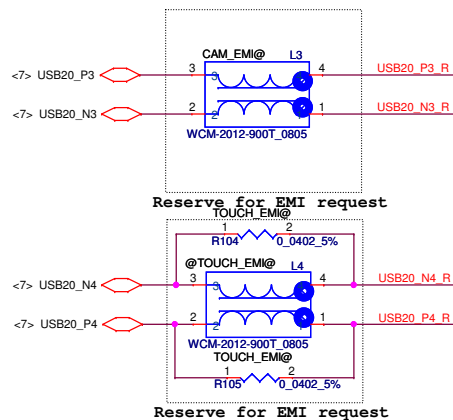
LCD Control



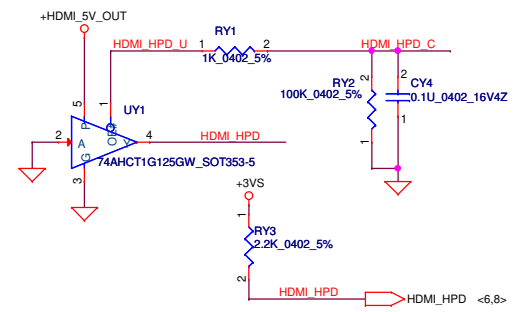
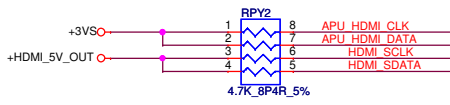
Reserve for eDP panel potential issue



Camera & Touch Screen



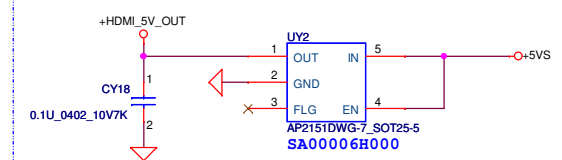
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	LVDS/EDP W/ CAMERA	
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					LA-9868P	1.0
				Date	Thursday, May 16, 2013	Sheet 20 of 42



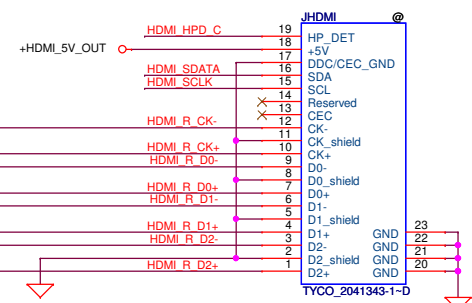
OE#	A	Y
L	L	L
L	H	H
H	X	Z

HDMI POWER CIRCUIT

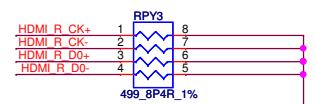
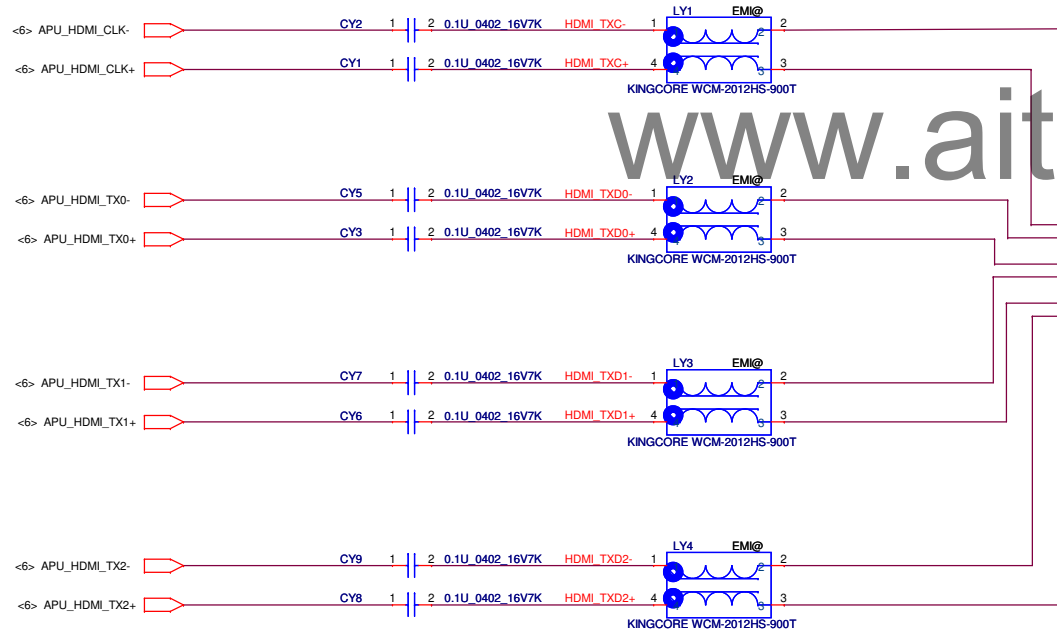
VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



HDMI Connector



www.aitech1.ru

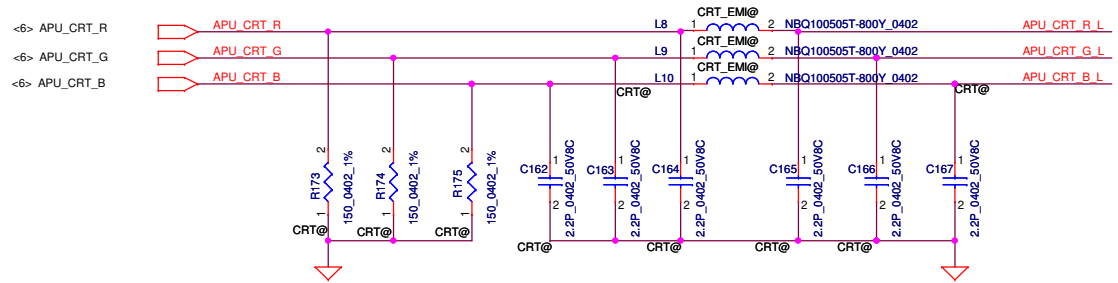


HDMI Royalty
HDMI W/O Logo + HDCP
RO0000003HM

HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

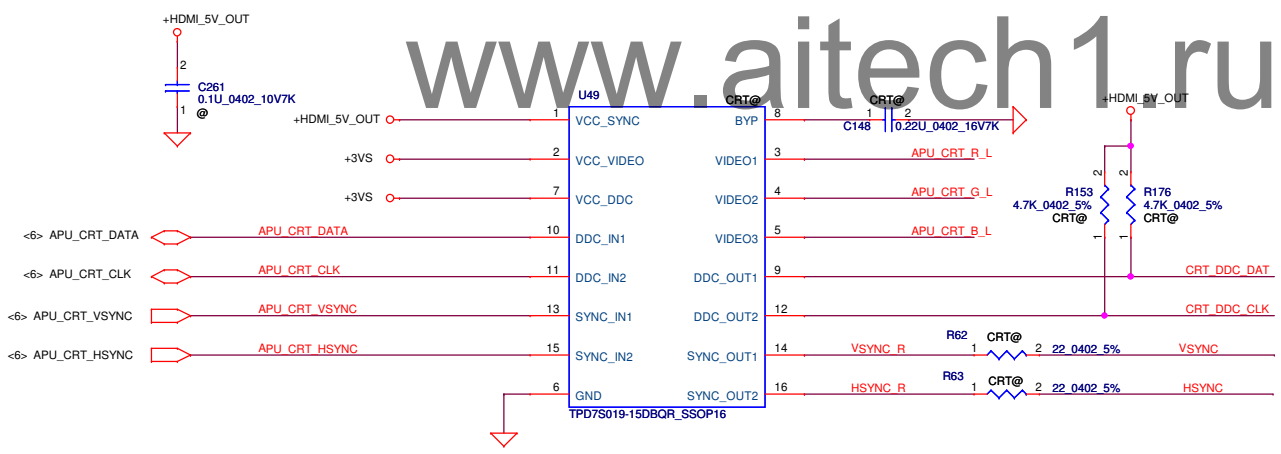
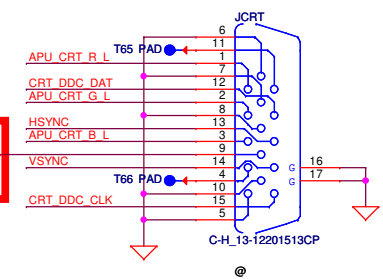
please manually load
this virtual material to 45@ BOM

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	HDMI W/O CEC
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					LA-9868P
				Date	Thursday, May 16, 2013
				Sheet	21 of 42
				Rev	1.0



+HDMI_5V_OUT

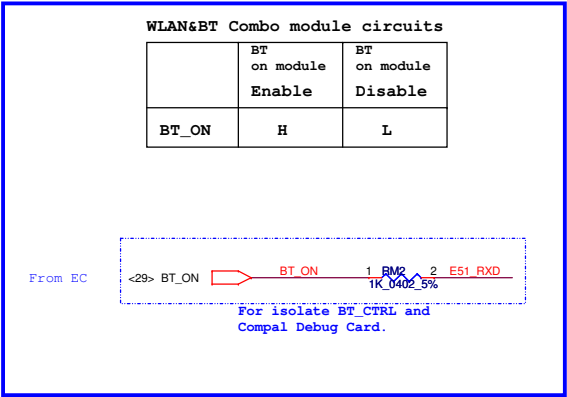
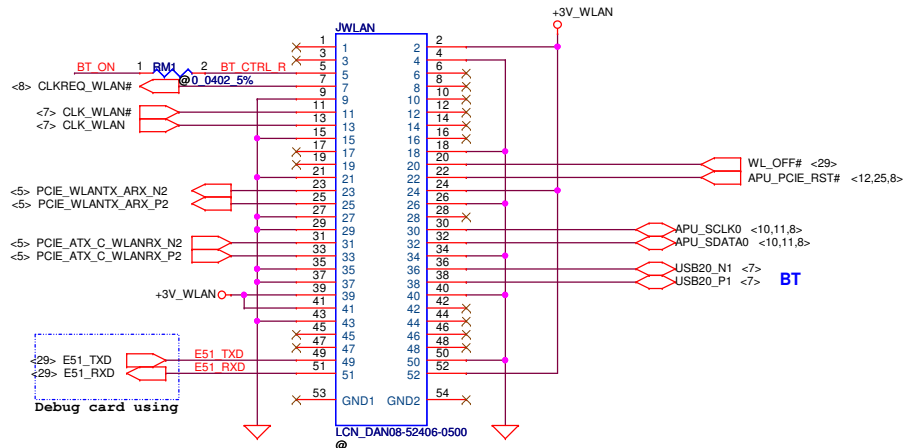
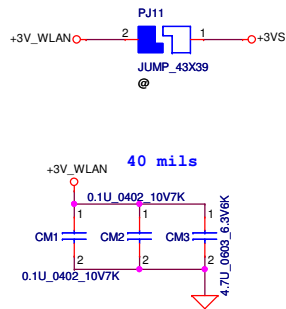
USE HDMI POWER



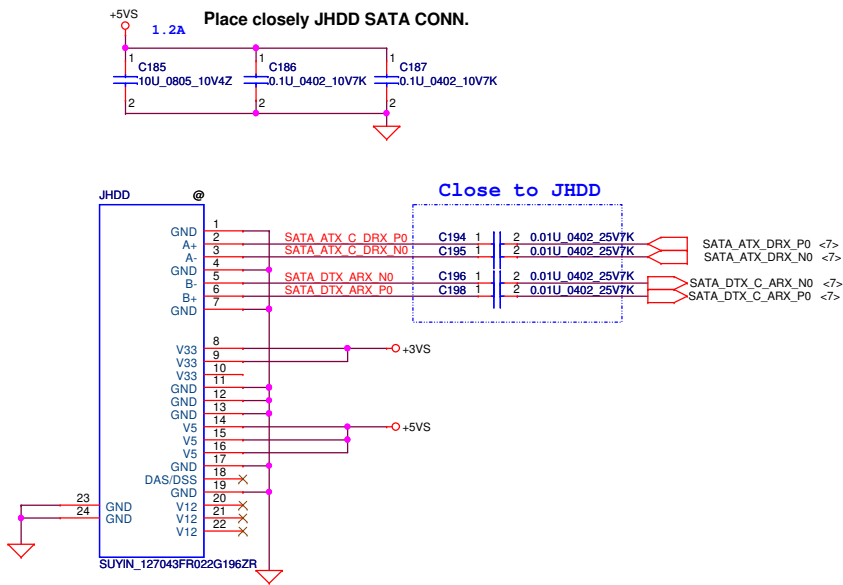
www.aitech1.ru

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	
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Size		Document Number			Rev
		LA-9868P			1.0
Date		Thursday, May 16, 2013			Sheet
		22			of 42

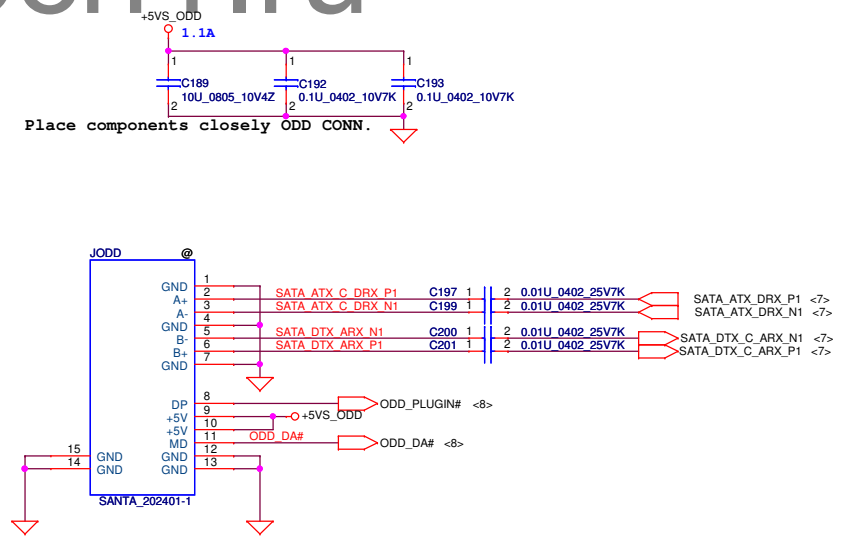
Slot 1 Half PCIe Mini Card-WLAN



SATA HDD Conn.

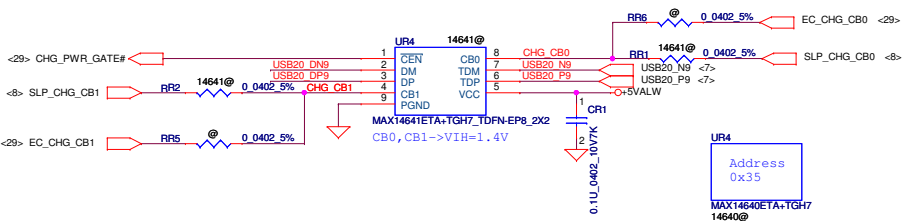


SATA ODD Conn

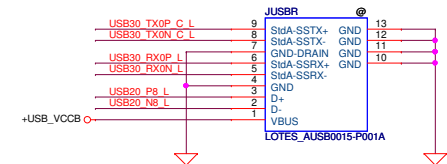
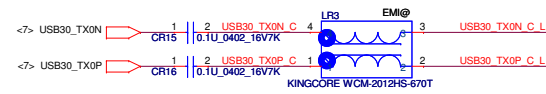
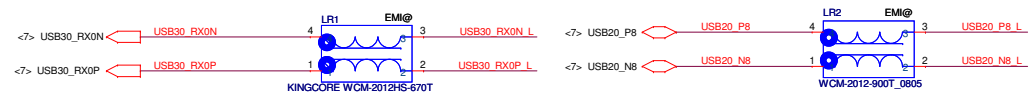


USB Sleep & Charge

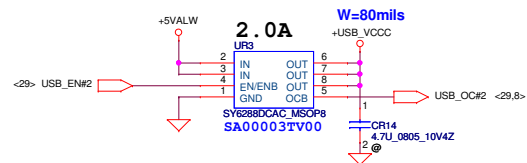
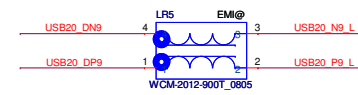
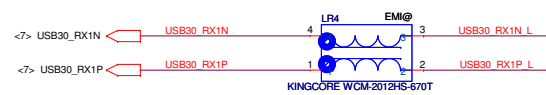
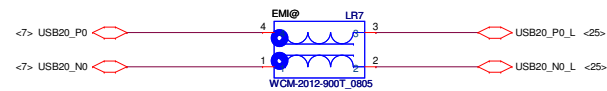
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



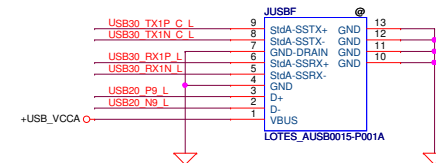
Right side USB 3.0 x 2/ Sleep&Charge



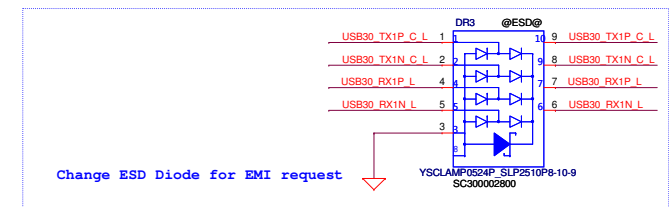
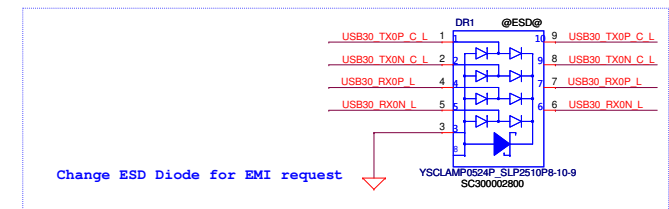
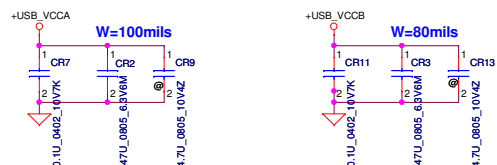
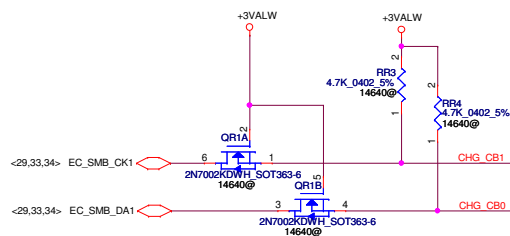
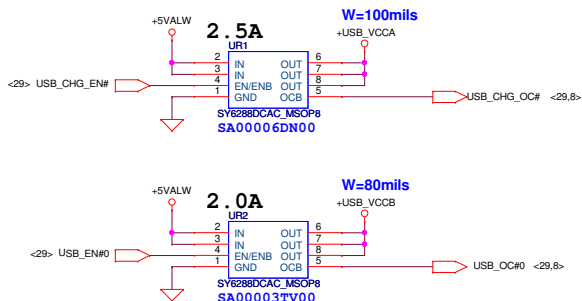
Left Side USB Port



Sleep & Charge Port

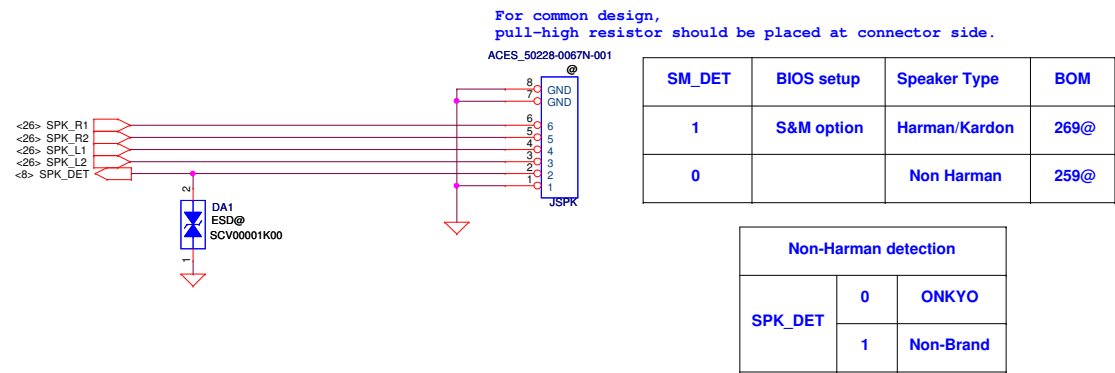


USB POWER SWITCH

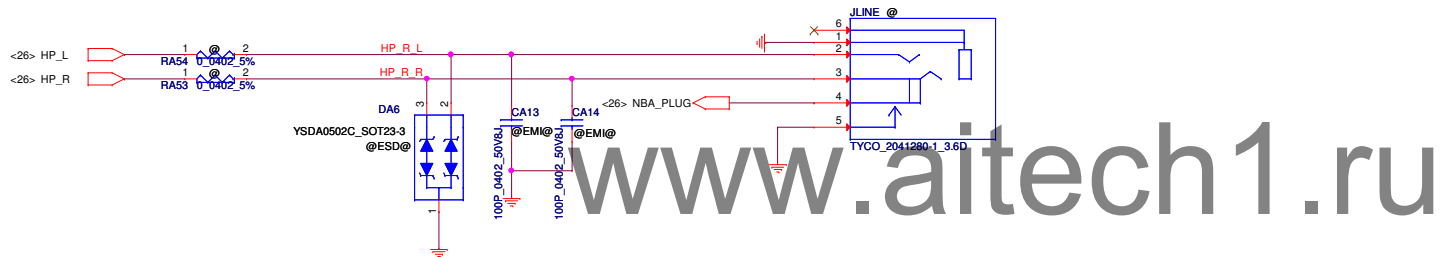


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	LUSB/RUSB/S&C	
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				LA-9868P	1.0	
Date: Thursday, May 16, 2013				Sheet	24	of 42

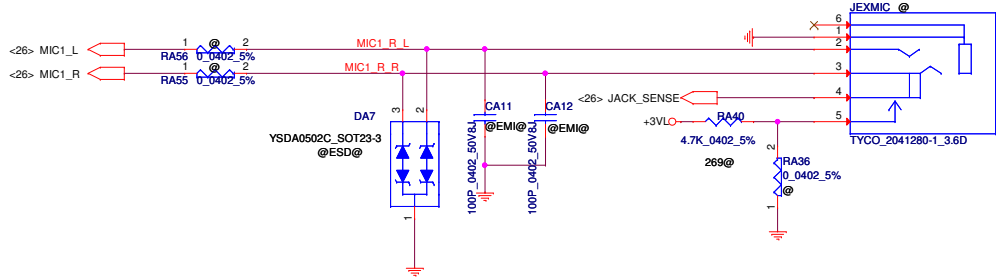
SPK Conn.

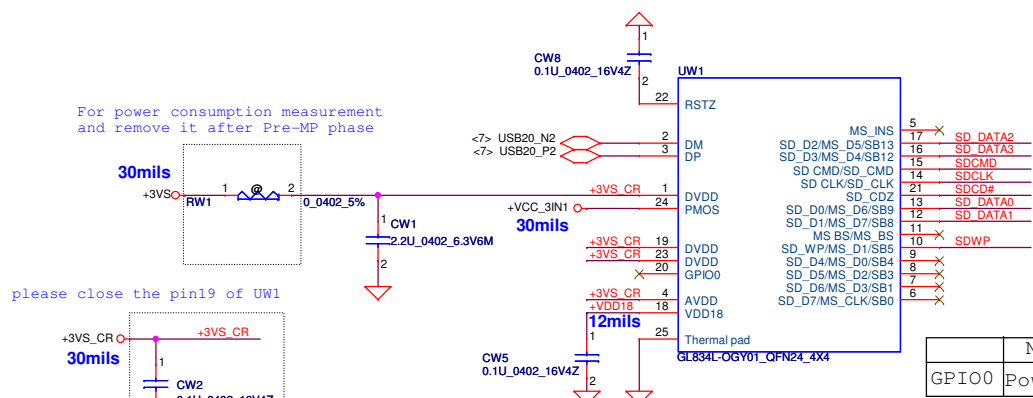


HeadPhone/LINE Out JACK

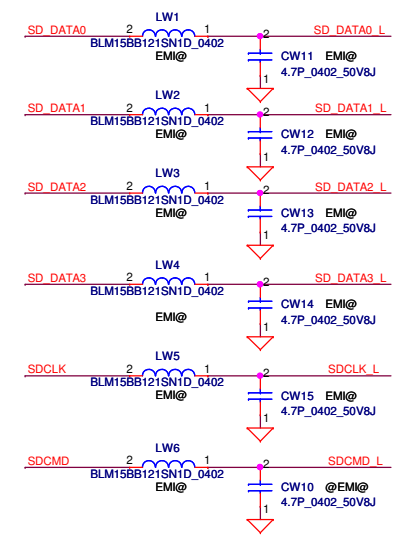
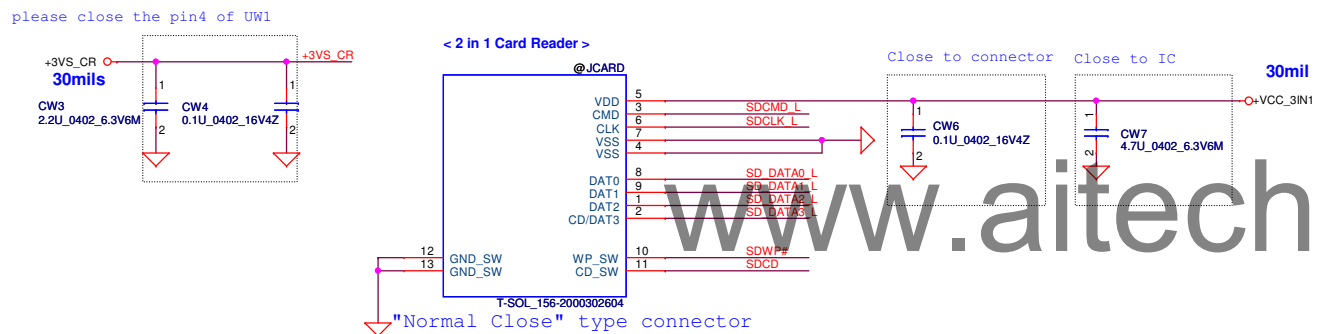


MIC/LINE IN JACK

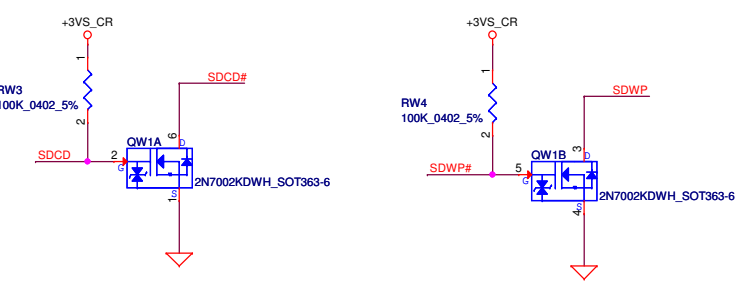


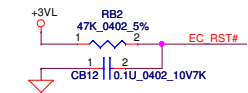
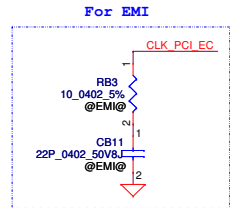


De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket

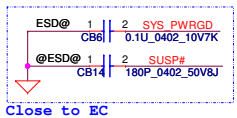
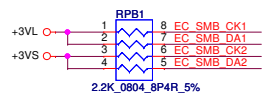


For normal close type connector invert circuit

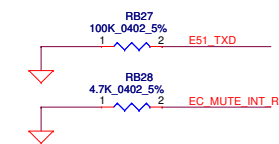




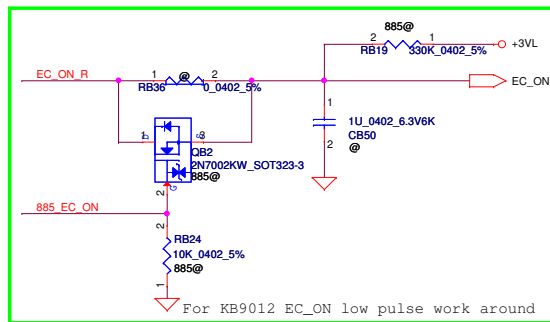
SMBUS1->BATT, Smart Charger
SMBUS2->G-Sensor, GPU Thermal Sensor,
APU Thermal Sensor
EC SMBus2 for S0, SMBus1 for S5



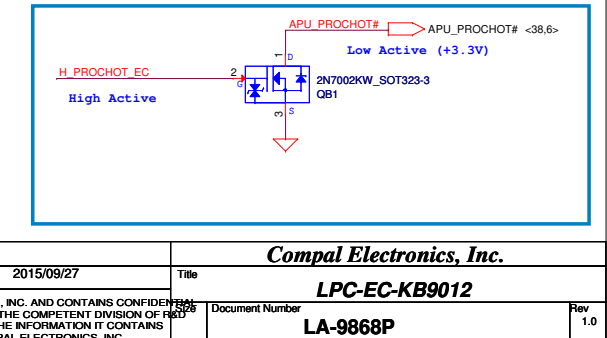
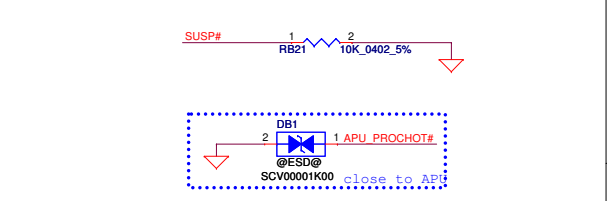
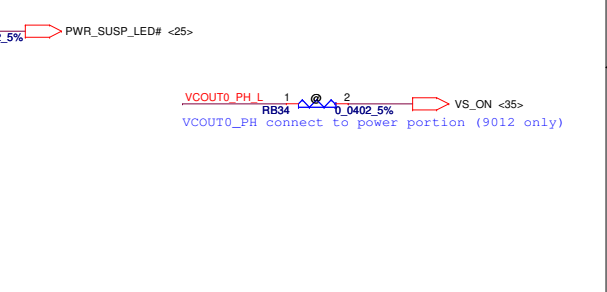
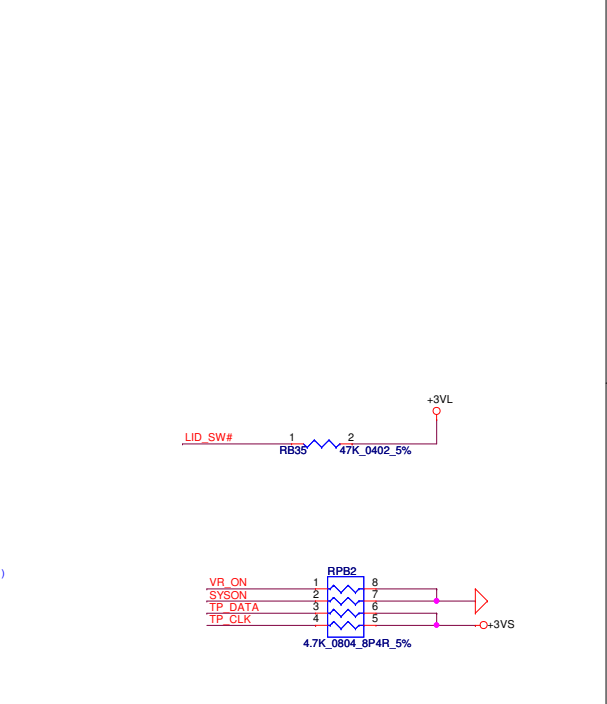
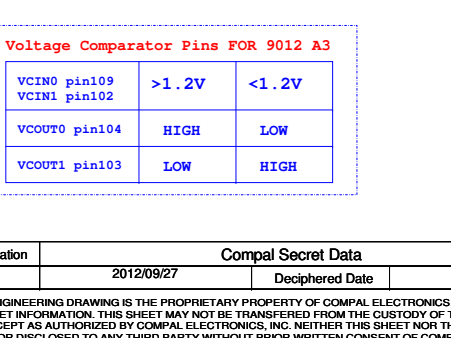
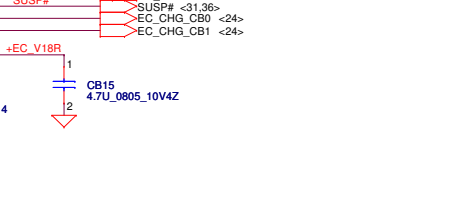
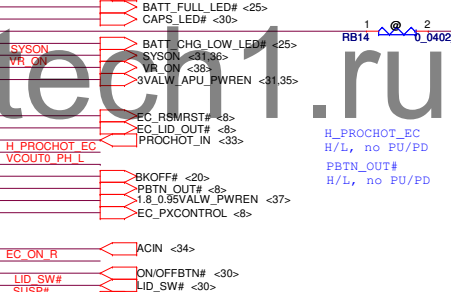
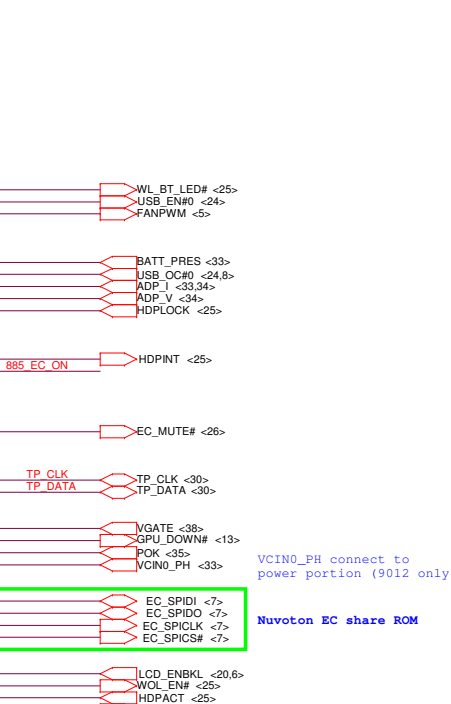
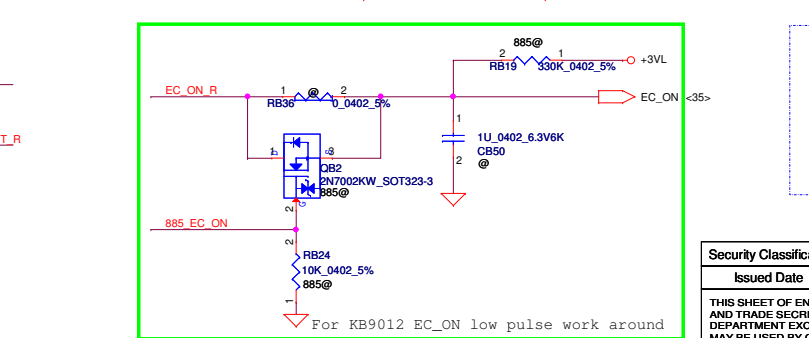
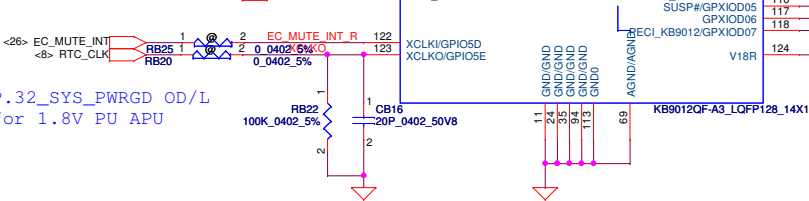
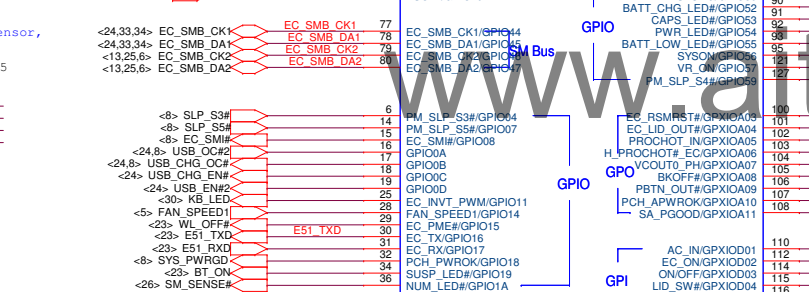
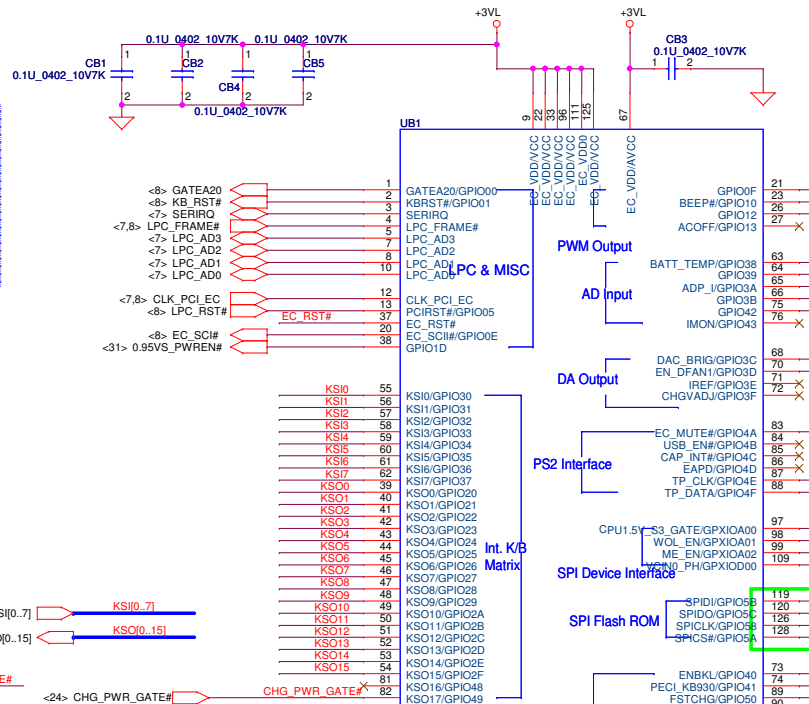
Close to EC



P.32_SYS_PWRGD OD/L
for 1.8V PU APU



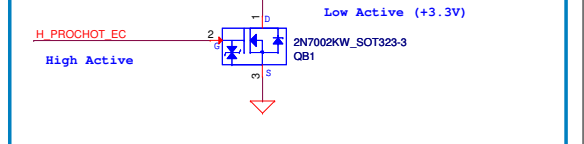
For KB9012 EC_ON low pulse work around



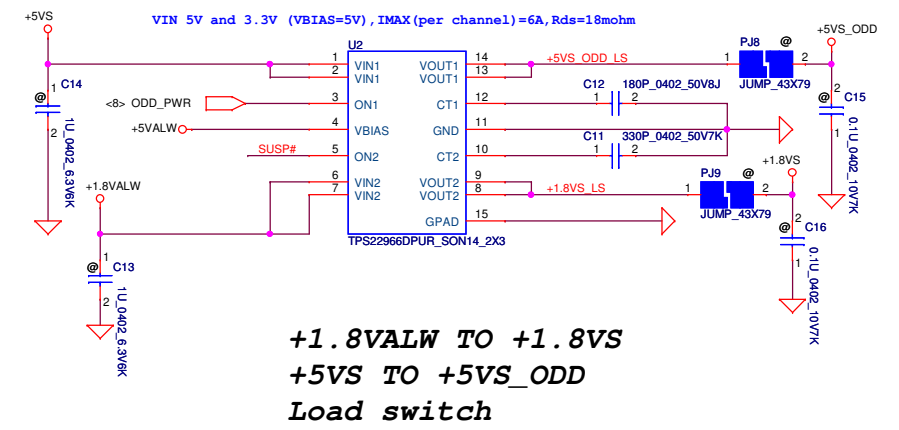
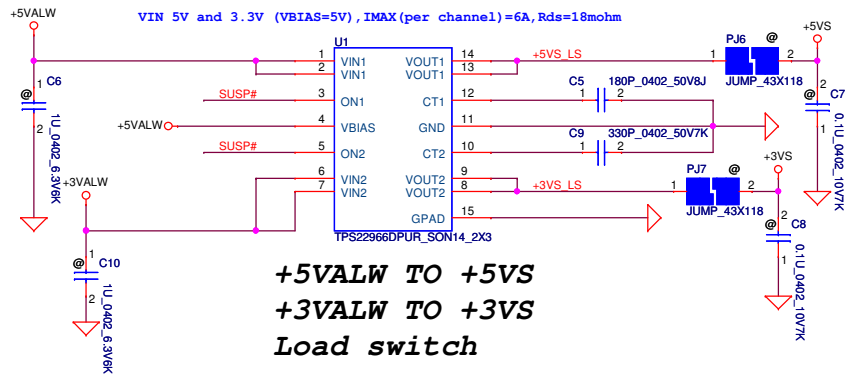
Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109	>1.2V	<1.2V
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH

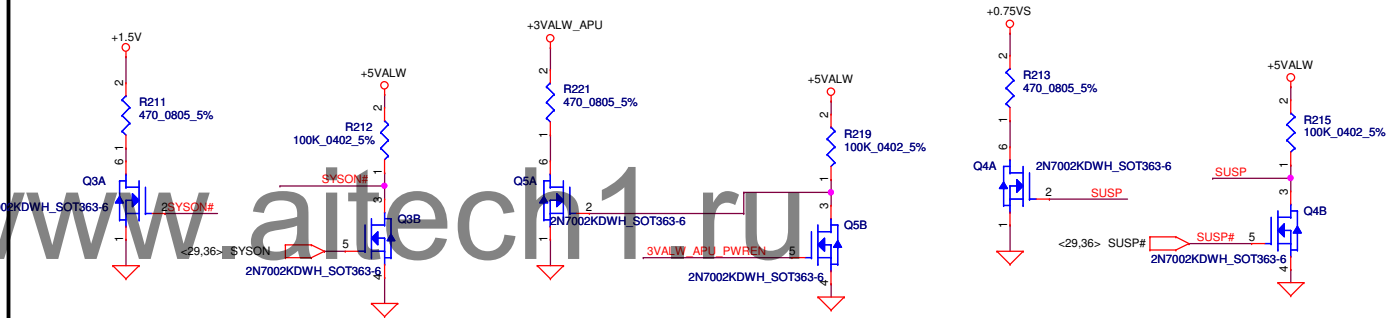
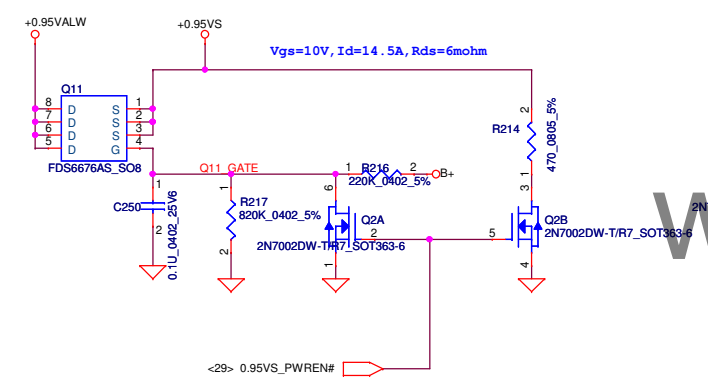
Security Classification	Compal Secret Data	
Issued Date	2012/09/27	Deciphered Date
2015/09/27		



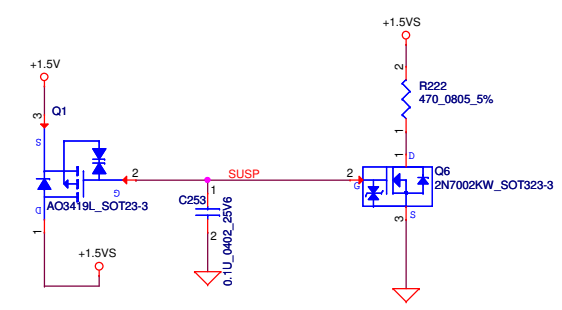
Compal Electronics, Inc.	
LPC-EC-KB9012	
Document Number	LA-9868P
Date	Thursday, May 16, 2013
Sheet	29 of 42



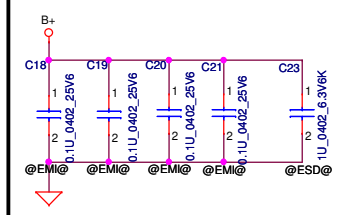
+0.95VALW to +0.95VS



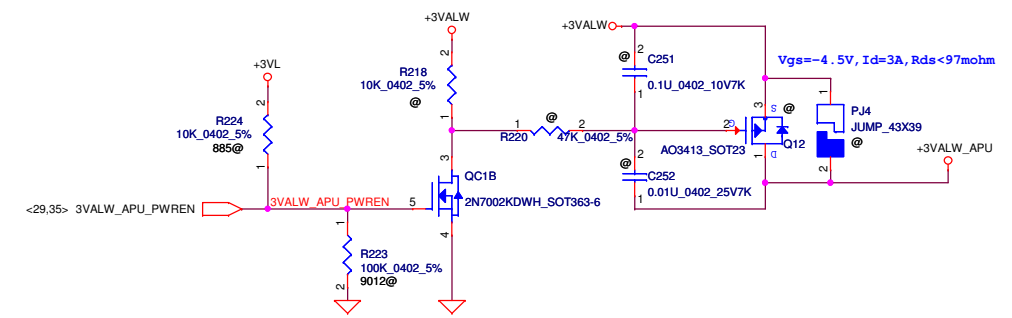
+1.5V to +1.5VS



EMI Cap.
Please check location



+3VALW to +3VALW_FCH

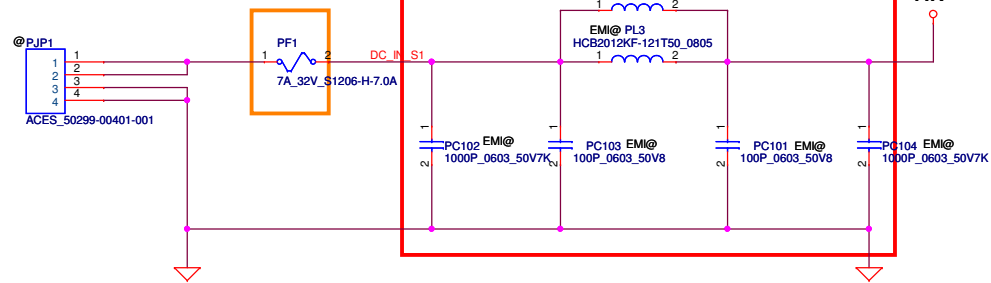


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	DC TO DC INTERFACE
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				LA-9868P	
				Date	Thursday, May 16, 2013
				Sheet	31 of 42

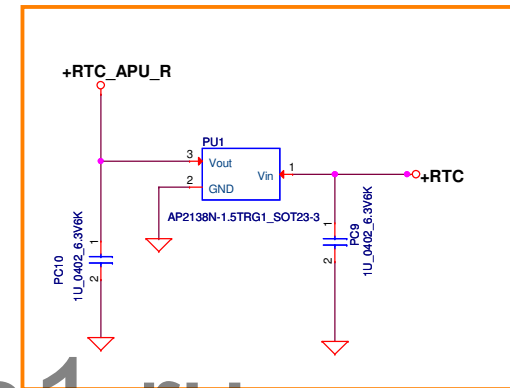
EMI Part (47.1)

Other component (37.1)

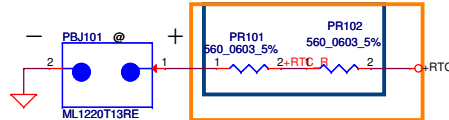
A51 need add fuse



For RTC (38.2)

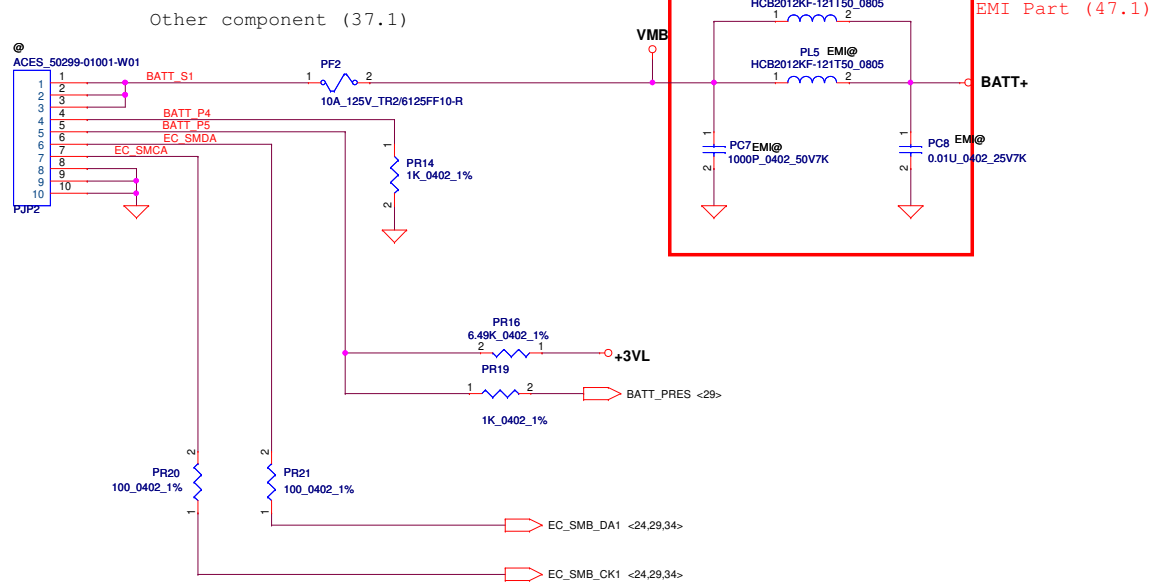


For ML1220 RTC (38.2)

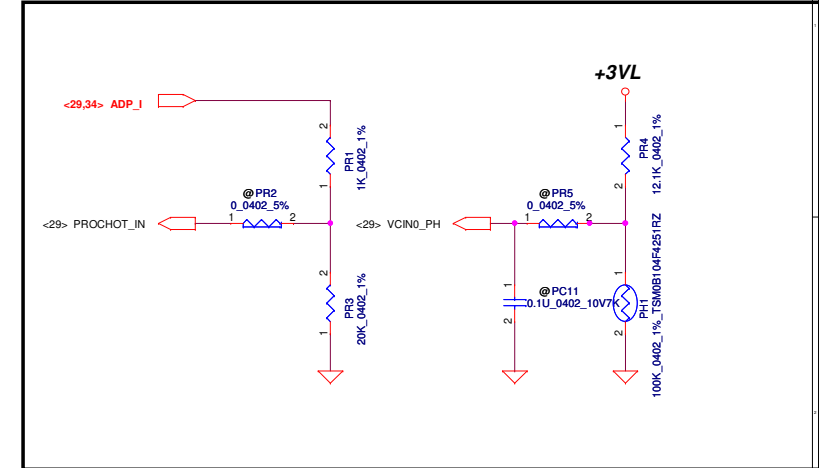


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Date:				Rev 1.0
Sheet 32 of 42				Document Number LA-9868P



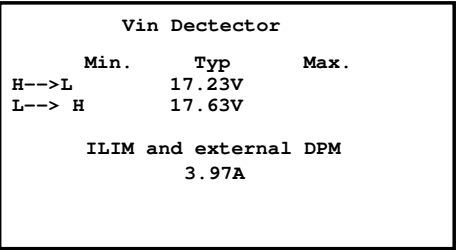
OTP (39.7)



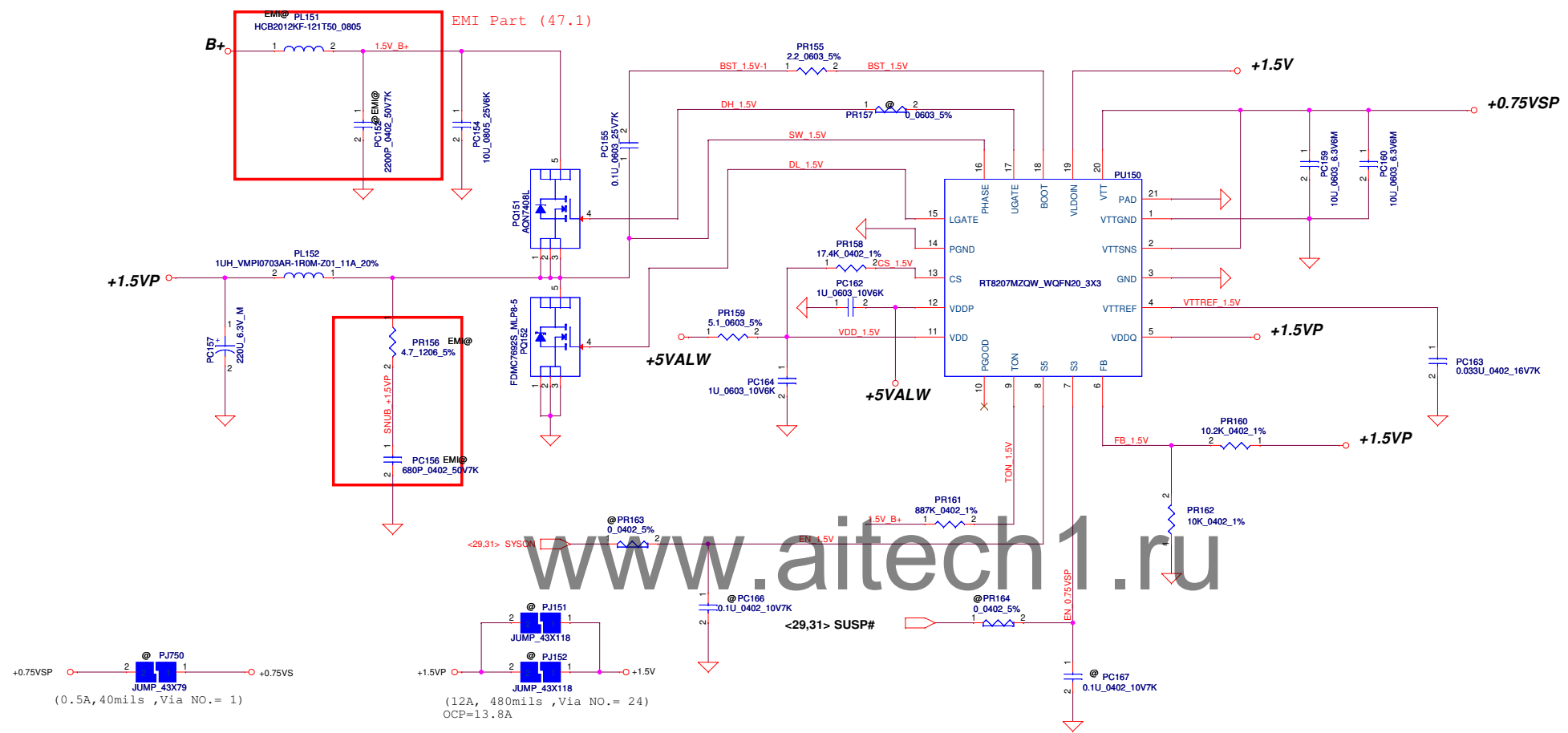
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				Document Number	LA-9868P
				Date:	Sheet 33 of 42

Charger controller (40.1), Support component (40.2)



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				Custom	LA-9868P	1.0
Date:				Sheet	34	of 42

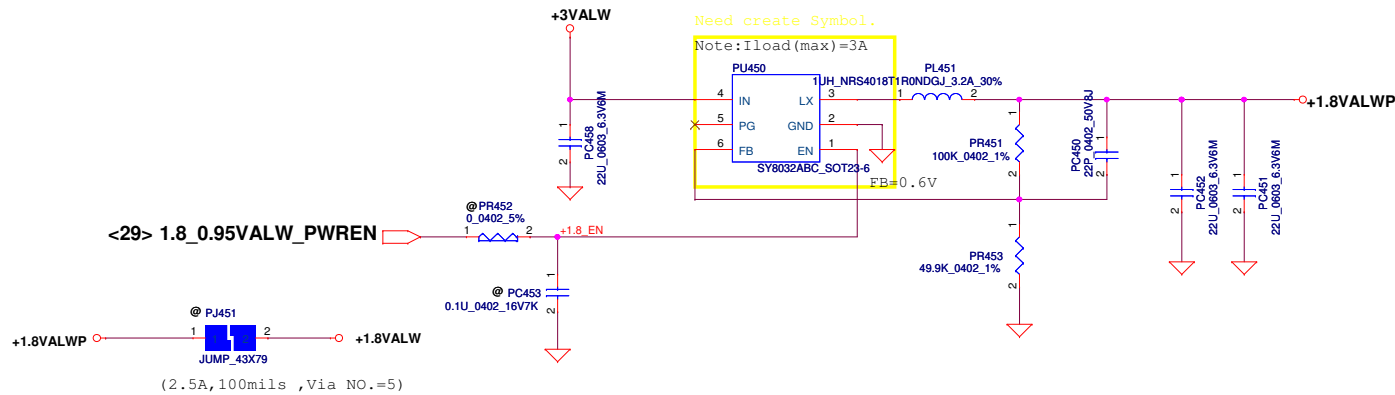


1.5V
Peak Current 12A
OCF current 13.82A
FSW=500kHz
DCR 8.3 ~ 10mohm
TYP MAX
H/S Rds (on) :27mohm , 34mohm
L/S Rds (on) :10.8mohm , 13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

1.8V controller (35.15), Support component (35.16)

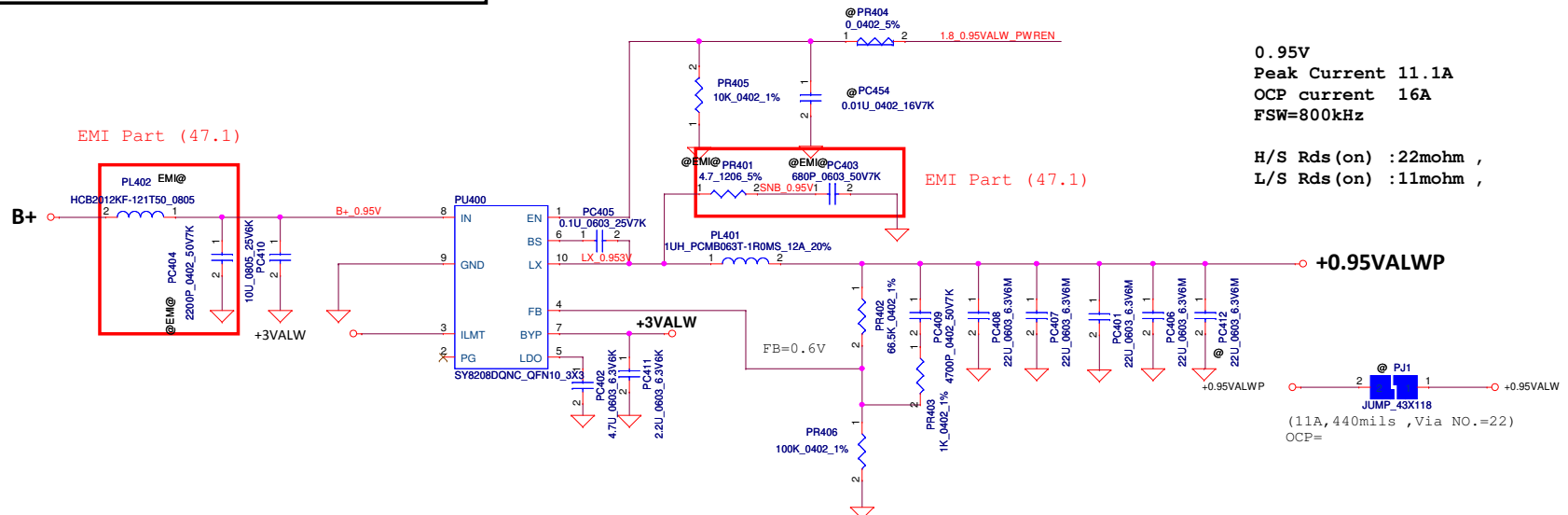


1.8V
Peak Current 2.5A
OCP current 3.5A
FSW=800kHz

H/S Rds(on) :100mohm ,
L/S Rds(on) :80mohm ,

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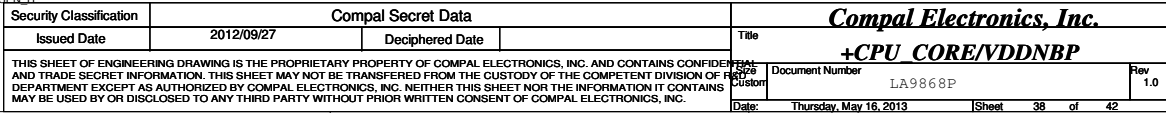
0.95V controller (35.5), Support component (35.6)



0.95V
Peak Current 11.1A
OCP current 16A
FSW=800kHz

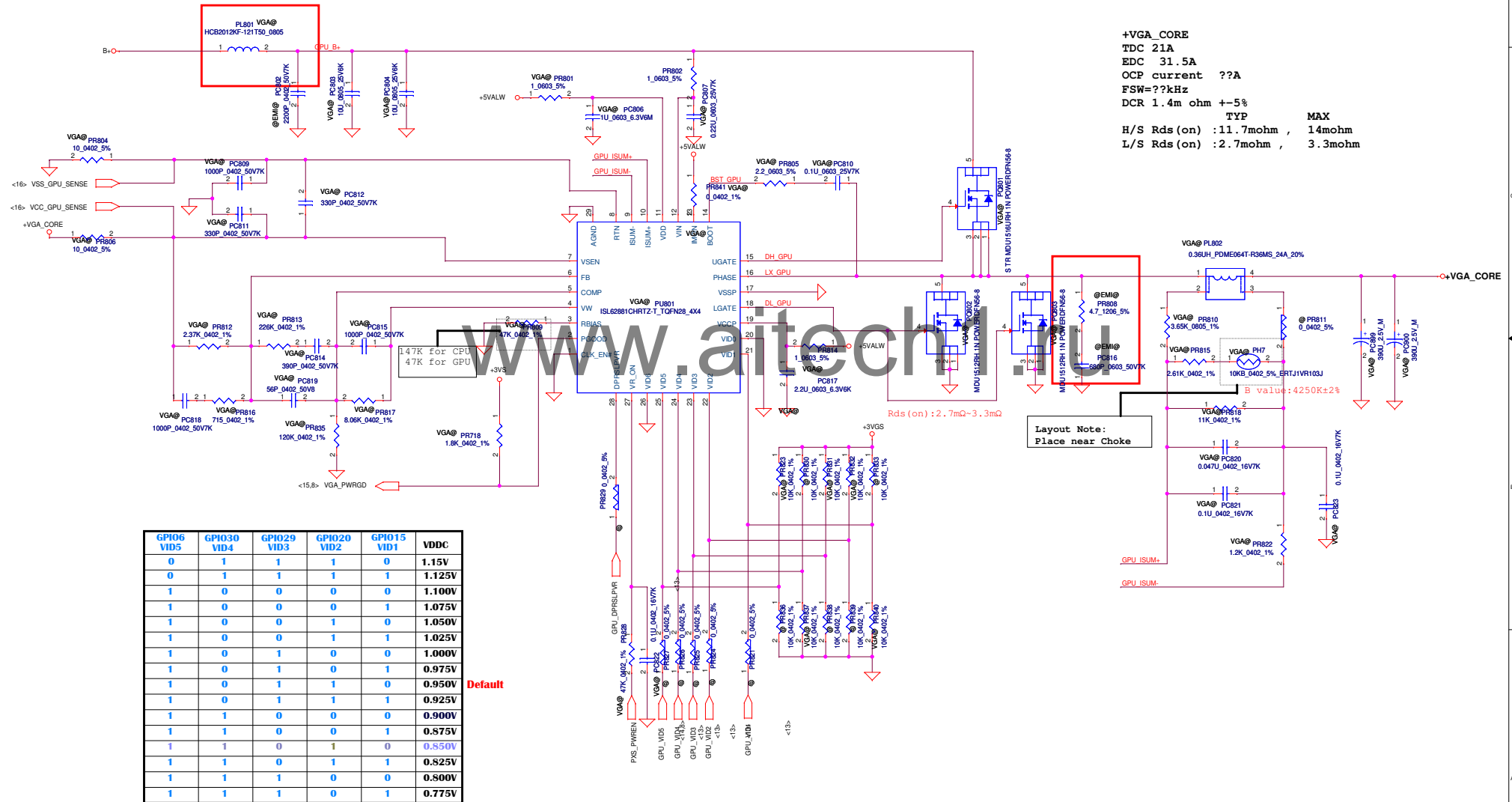
H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

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Size		Document Number		Rev	
Custom		LA-9868P		1.0	
Date:		Thursday, May 16, 2013		Sheet 37 of 42	



VGA controller (43.1),Driver (43.2) Support component (43.3)

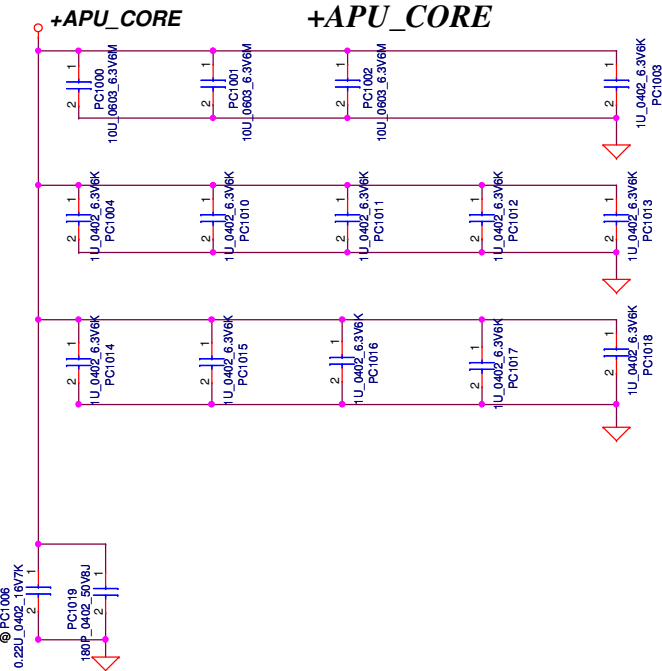
EMI Part (47.1)



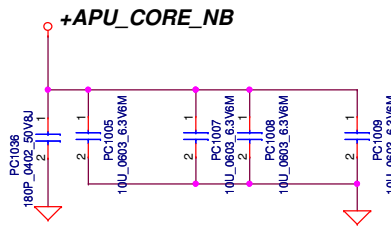
GPIO6 VID5	GPIO30 VID4	GPIO29 VID3	GPIO20 VID2	GPIO15 VID1	VDDC
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

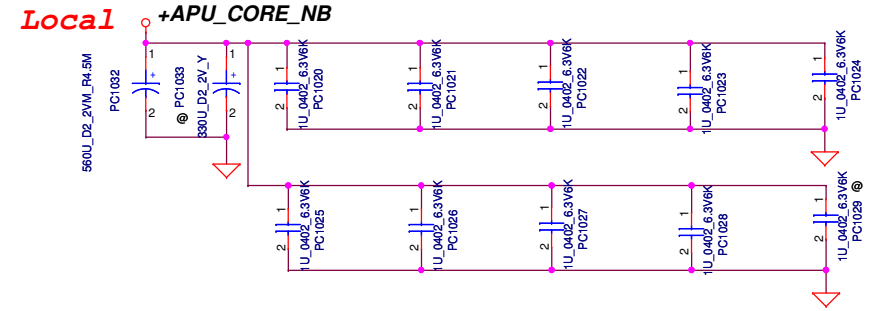
CPU_Core output CAP (Including MLCC) 36.4



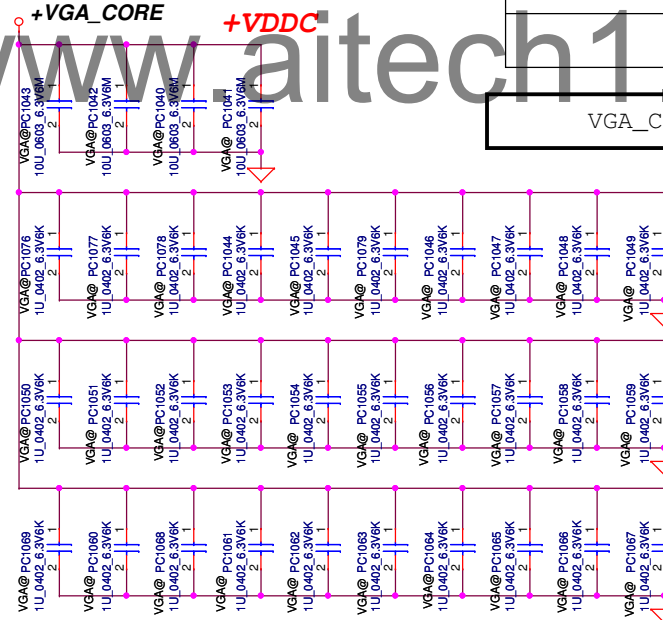
+APU_CORE_NB



GFX output CAP (Including MLCC) 36.5



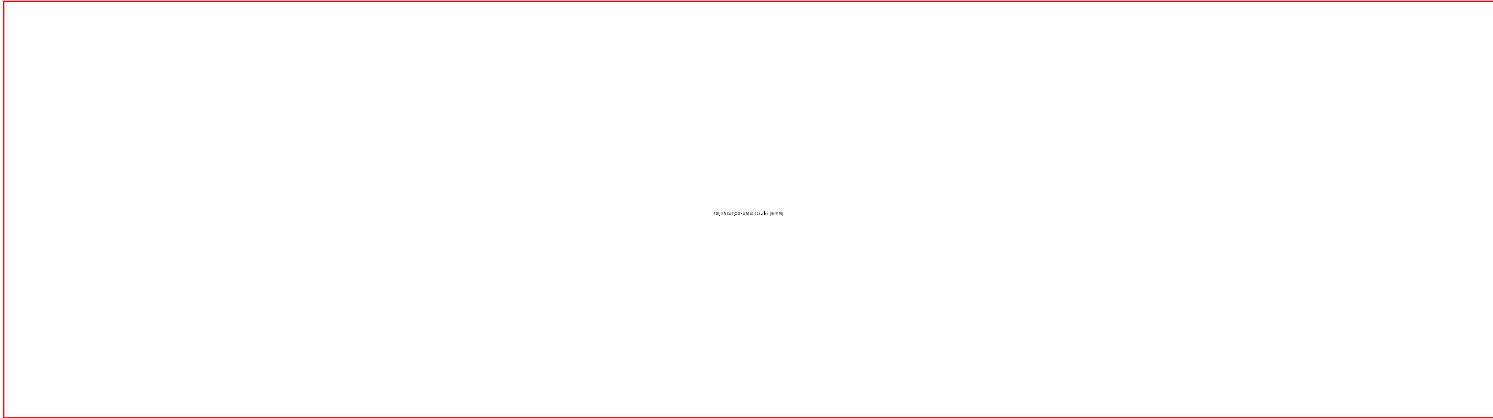
+VGA_CORE



VGA_Core output CAP (Including MLCC) 43.9

kabini	560uF*4.5m	10uF (0603)	1u (0402)	0.22uF	180P (0402)
VDD	2	3	11		1
VDD_NB	1	4	9		1

Item	Reason for change	PG#	Modify List	Date	Phase
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				Date: Thursday, May 16, 2013	Rev 1.0
				Sheet 41 of 42	

HW PIR (Product Improve Record)

VNKAE LA-9868P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

Item	Page	Date	Request	Solution
1		2013/03/5a	Change APU to PR sample	PR sample PN SA00006R300, SKU 4519NL51L03
2	P30	2013/03/5a	PCB cut outline	Remove SW1
3	P06	2013/03/5a	co-lay eDP & LVDS	Due to common eDP cable, swap Lane0 and Lane2 to follow common design; replace CC106, CC102 with RC75, RC76; add RC77, RC78, CC109, CC110.
4	P30	2013/03/06a	no need power button	Remove SW2
5	P30	2013/03/06a		Add C24(0.1uF) to ON/OFFBIN# and set to ESD@
6	P06	2013/03/06a		Add CC99(1000pF) to APU_RST# and set to ESD@
7		2013/03/06a		Change CC93, CC94, CC97, CB6 to ESD@
8	P07	2013/03/06a	BIOS ROM	Change UC5 to always mount on 43-level
9	P07	2013/03/06a	For vendor recommand	Change CC22, CC23 from 5.6pF to 4.7pF(SE07147AC80)
10	P28	2013/03/07a	co-lay card reader for EMI request	Update card reader schematic for co-lay GL834L and RT5117
11	P09	2013/03/07b	Remove 0ohm res	Change RC116, RC117, RC119, RC120 to short pad symbol
12	P26	2013/03/07b	Remove 0ohm res	Change RA18, RA24, RA22, RA36, RA37 to short pad symbol
13	P05	2013/03/07b	Remove 0ohm res	Change R2 to short pad symbol
14	P20	2013/03/07b	Remove 0ohm res	Remove R106
15	P29	2013/03/07b	Remove 0ohm res	Change RB36 to short pad symbol
16		2013/03/11a	Update power schematic	
17	P28	2013/03/12a	Remove co-lay RT5117	Update card reader schematic
18	P30	2013/03/18a	Change PCB PN	Change PCB PN to DAZ0WJ00100
19	P30	2013/03/18a		Remove DC-IN JACK PN due to BOM structure changed
20	P24	2013/03/18a	Remove 0ohm res	Change RR1, RR2 to short pad symbol
21	P08	2013/03/18a	For power consumption improve	Change VRAM_SEL to TOUCH_SEL for BTO to improve battery life.
22	P26	2013/03/25a	ESD request	Change DA1, CA30, CA31, CA34, CA36 to varistor(SCV00001K00)
23	P08	2013/03/25a	vendor recommand	Change CC31 to 8pF(SE00000DB80)
24	P24	2013/03/25a	Remove 0ohm res	Change RR1, RR2 to 0 ohm

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Title			HW PIR
Size	Document Number	Rev	
B	LA-9868P	1.0	
Date:	Thursday, May 16, 2013	Sheet	42 of 42